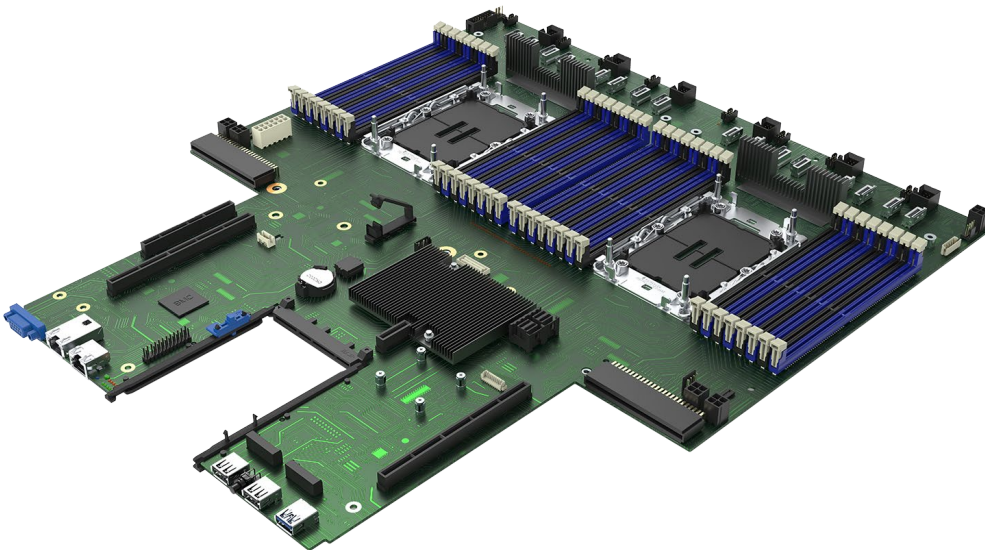# Intel® Server Board M50FCP2SBSTD

Technical Product Specification

An overview of product features, functions, architecture, and support specifications.

Rev. 1.0

January 2023

M50FCP2S

Delivering Breakthrough Data Center System Innovation – Experience What's Inside!

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Document Revision History

Date	Revision	Changes
January 2023	1.0	Production Release

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1.   Introduction

This technical product specification (TPS) provides a high-level overview of the features, functions, architecture, and support specifications of the Intel® Server Board M50FCP2SBSTD.

The board is a monolithic printed circuit board assembly with features that are intended for high density rack mount server systems. These server boards are designed to support the 4th Gen Intel® Xeon® Scalable processor family. Previous generations of the Intel® Xeon® processor and Intel® Xeon® Scalable processor families are not supported.

The Intel® Server Board M50FCP2SBSTD is a foundational building block of the server system. The server board is backed by Intel® design excellence, manufacturing expertise, and world-class support to deliver processing power with high levels of flexibility, manageability, and reliability.

Notes:
- This document includes several references to Intel® websites where additional product information can be downloaded. However, these public Intel sites do not include content for products in development. Content for these products is available on the public Intel websites after their public launch.
- In this document, the 4th Gen Intel® Xeon® Scalable processor family may be referred to simply as "processor".
- In this document, DDR5 DIMM and Intel® Optane™ PMem devices are commonly referred to as "memory module".
- For more in-depth technical information, see the related documents in Section 1.1. Some of the documents listed in the section are classified as "Intel Confidential". These documents are made available under a nondisclosure agreement (NDA) with Intel and must be requested through your local Intel representative.
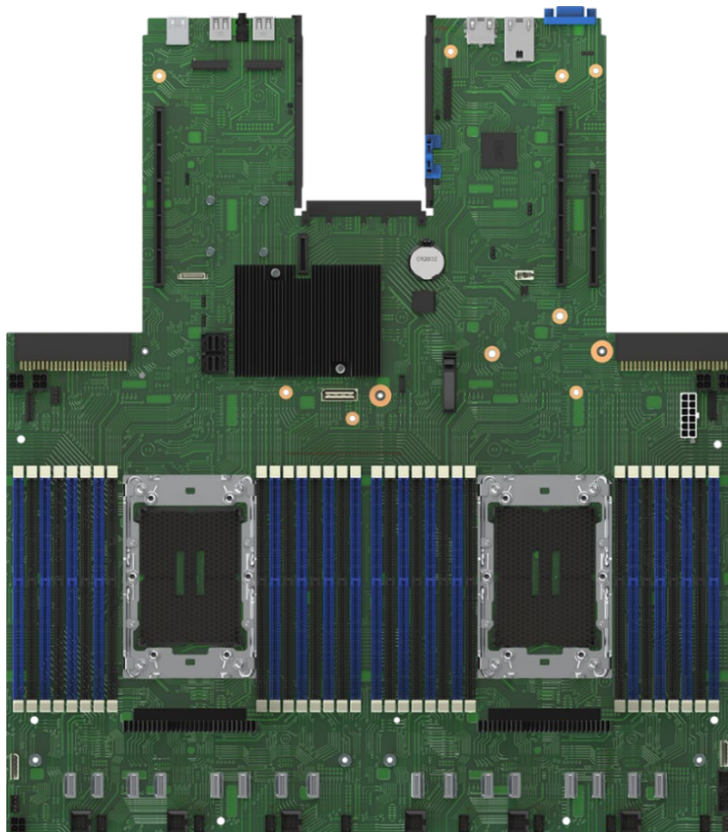
Figure 1. Intel® Server Board M50FCP2SBSTD

1.1   Reference Documents

For additional information, see the product support collaterals specified in the following table.

Table 1. Intel® Server M50FCP Family Reference Documents and Support Collaterals

Topic	Document Title or Support Collateral	Document Classification
System integration instructions and service guidance	*Intel® Server System M50FCP2UR System Integration and Service Guide*	Public
System integration instructions and service guidance	*Intel® Server System M50FCP1UR System Integration and Service Guide*	Public
Technical system-level description	*Intel® Server System M50FCP2UR Technical Product Specification*	Public
Technical system-level description	*Intel® Server System M50FCP1UR Technical Product Specification*	Public
Technical board-level description	*Intel® Server Board M50FCP2SBSTD Technical Product Specification*	Public
Server configuration guidance and compatibility	*Intel® Server M50FCP Family Configuration Guide*	Public
Information on the Integrated BMC Web Console	*Integrated Baseboard Management Controller Web Console (Integrated BMC Web Console) User Guide*	Public
BIOS technical information on product family	4th Gen Intel® Xeon® Scalable processors family *BIOS Firmware External Product Specification (EPS)*	Intel Confidential
BIOS setup information on product family	*BIOS Setup Utility User Guide*	Public
BMC technical information on product family	*Integrated Baseboard Management Controller Firmware External Product Specification (EPS)*	Intel Confidential
Base specifications for the IPMI architecture and interfaces	*Intelligent Platform Management Interface Specification Second Generation v2.0*	Intel Confidential
Specifications for the PCIe* 3.0 architecture and interfaces	*PCIe Base Specification, Revision 3.0* http://www.pcisig.com/specifications	Public
Specifications for the PCIe* 4.0 architecture and interfaces	*PCIe Base Specification, Revision 4.0* http://www.pcisig.com/specifications	Public
Specifications for the PCIe* 5.0 architecture and interfaces	*PCIe Base Specification, Revision 5.0* http://www.pcisig.com/specifications	Public
Specification for OCP*	Open Compute Project (OCP) Specification	Public
TPM for PC Client specifications	*TPM PC Client Specifications, Revision 2.0*	Intel Confidential
Functional specifications of 4th Gen Intel® Xeon® Scalable processor family	*Sapphire Rapids External Design Specification (EDS):* Document IDs: 630161, 612246, 612172, 633350, 611488	Intel Confidential
Processor thermal design specifications and recommendations	*Sapphire Rapids Thermal and Mechanical Specifications and Design Guide (TMSDG)*: Document ID 609847	Intel Confidential
BIOS and BMC security best practices	*Intel® Server Systems Baseboard Management Controller (BMC) and BIOS Security Best Practices White Paper* *https://www.intel.com/content/www/us/en/support/articles/000055785/server-products.html*	Public
Managing an Intel® server overview	*Managing an Intel® Server System 2020* *https://www.intel.com/content/www/us/en/support/articles/000057741/server-products.html*	Public
Technical information on Intel® Optane™ PMem 300 series	*Intel® Optane™ Persistent Memory 300 Series Operations Guide*	Intel Confidential
Setup information for Intel® Optane™ PMem 300 series	*Intel® Optane™ Persistent Memory Startup Guide*	Public
Latest system software updates: BIOS and firmware	*Intel® System Update Package (SUP) for Intel® Server M50FCP Family*	Public
	Intel® Server Firmware Update Utility - Various operating system support	
	Intel® Server Firmware Update Utility User Guide	
	Intel® Server Information Retrieval Utility - Various operating system support	Public

Topic	Document Title or Support Collateral	Document Classification
To obtain full system information	*Intel® Server Information Retrieval Utility User Guide*	
To configure, save, and restore various system options	*Intel® Server Configuration Utility – Various operating system support*	Public
	Intel® Server Configuration Utility User Guide	
Product warranty information	*Warranty Terms and Conditions* https://www.intel.com/content/www/us/en/support/services/000005886.html	Public
Intel® Data Center Manager (Intel® DCM) information	*Intel® Data Center Manager (Intel® DCM) Product Brief* *Intel® Data Center Manager (Intel® DCM) Product Brief*	Public
	Intel® Data Center Manager (Intel® DCM) Console User Guide *Intel® Data Center Manager (Intel® DCM) Console User Guide*	Public

Note: Intel Confidential documents are made available under an NDA with Intel and must be ordered through a local Intel representative.

2. Server Board Family Overview

This chapter identifies the board's features and functions, provides mechanical dimensional diagrams, and an overview of each board architecture.

2.1 Server Board Feature Set

The following table provides a high-level overview of the Intel® Server Board M50FCP2SBSTD.

Table 2. Intel® Server Board M50FCP2SBSTD Features

Feature	Details
Server Board	Intel® Server Board M50FCP2SBSTD
Server Board Dimensions	18.9" (480 mm) length x 16.9" (428 mm) width

Processor Support	• Dual Socket E LGA4677
	• Supported 4th Gen Intel® Xeon® Scalable processor family SKUs:
	  o Intel® Xeon® Platinum 84xxxx processor
	  o Intel® Xeon® Gold 64xxxx processor
	  o Intel® Xeon® Gold 54xxxx processor
	  o Intel® Xeon® Silver 44xxxx processor
	  o Intel® Xeon® Bronze 34xxxx processor
	• Intel® UPI links: 3 @ 16 GT/s (Platinum and Gold families) or 2 @ 16 GT/s (Silver family)
	Notes:
	• Intel® Xeon® Bronze processors are used in single processor configurations only.
	• Previous generations of Intel® Xeon® processors are not supported.

Maximum Supported Processor Thermal Design Power (TDP)	• Up to 350 W **Note:** The maximum supported processor TDP at the system level may be lower than what the server board can support. Supported power, thermal, and configuration limits of the chosen server chassis need to be considered to determine if the system can support the maximum processor TDP limit of the server board. Refer to the server chassis/system documentation for additional guidance.

Chipset PCH	• Intel® C741 chipset platform controller hub (PCH)
	• Embedded features enabled on this server board:
	  o SATA 3.0 support
	  o USB 3.0 support
	  o PCIe 3.0 support

Server Management Processor (SMP	• ASpeed* AST2600 Advanced PCIe Graphics and Remote Management Processor
	• Embedded features enabled on this server board:
	  o Baseboard Management Controller (BMC)
	  o 2D Video Graphics Adapter

Memory Support	• 32 memory slots total
	  o 8 memory channels per processor
	  o 2 memory slots per channel
	• Registered SDRAM DDR5 DIMMs (RDIMM, 3DS-RDIMM, and 9x4 RDIMM)
	Note: 3DS = 3-dimensional stacking.
	• All DIMMs must support ECC
	• Intel® Optane™ PMem 300 series (App Direct Mode only)
	• Memory capacity: Up to 12 TB per processor (processor SKU dependent) using DDR5 RDIMMs combined with Intel® Optane™ PMem 300 series modules
	• Up to 4800 MT/s at one RDIMM per channel (processor SKU dependent)

Feature	Details
	• Up to 4400 MT/s at two RDIMMs per channel (processor SKU dependent) • DDR5 standard voltage of 1.1 V
System Fan Support	• Six 6-pin managed fan connectors • Eight 8-pin managed fan connectors • Two 4-pin managed CPU fan headers (one for each CPU)
Onboard Network Support	• Provided by optional Open Compute Project (OCP*) module support.
Open Compute Project (OCP*) Module Support	• Server board x16 PCIe 5.0 OCP 3.0 connector (Small Form-Factor) slot. Refer to https://servertools.intel.com/sct for the latest list of adapters supported by the server board.

Riser Card Support	Concurrent support for up to three riser cards with support for up to eight PCIe add-in cards.
	
	 In the following description FH = Full Height, FL = Full Length, HL =Half Length, LP = Low Profile.
	
	 Riser Slot #1
	 • Riser Slot #1 supports x32 PCIe lanes, routed from CPU 0
	 • PCIe 5.0 support for up to 64 GB/s
	 Riser Slot #1 supports the following Intel riser card options:
	 • Two PCIe slot riser card (iPC **FCP2URISER1DW**), which supports:
	     o One FH/FL double-width slot (x16 electrical, x16 mechanical)
	     o One FH/HL single-width slot (x16 electrical, x16 mechanical
	 • Two PCIe slot riser card (iPC **FCP2URISER1SW**), which supports:
	     o Two FH/FL single-width slot (x16 electrical, x16 mechanical)
	 • Three PCIe slot riser card (iPC **FCP2URISER1STD**), which supports:
	     o One FH/FL single-width slot (x16 electrical, x16 mechanical)
	     o One FH/FL single-width slot (x8 electrical, x16 mechanical)
	     o One FH/HL single-width slot (x8 electrical, x8 mechanical)
	 • NVMe riser card (iPC **FCP2URISER1RTM**), which supports:
	     o One FH/FL single-width slot (x16 electrical, x16 mechanical)
	     o Two x8 PCIe NVMe MCIO connectors, each with a retimer
	 • One PCIe slot riser card (iPC **FCP1URISER1**), which supports:
	     o One LP/HL, single-width slot (x16 electrical, x16 mechanical)
	
	 Riser Slot #2
	 • Riser Slot #2 supports x32 PCIe lanes, routed from CPU 1
	 • PCIe 5.0 support for up to 64 GB/s
	 Riser Slot #2 supports the following Intel riser card options:
	 • Two PCIe slot riser card (iPC FCP2URISER2DW), which supports:
	     o One FH/FL double-width slot (x16 electrical, x16 mechanical)
	     o One FH/HL single-width slot (x16 electrical, x16 mechanical)
	 • Two PCIe slot riser card (iPC **FCP2URISER2SW**), which supports:
	     o Two FH/FL single-width slot (x16 electrical, x16 mechanical)
	 • Three PCIe slot riser card (iPC **FCP2URISER2STD**), which supports:
	     o One FH/FL single-width slot (x16 electrical, x16 mechanical)
	     o One FH/FL single-width slot (x8 electrical, x16 mechanical)
	     o One FH/HL single-width slot (x8 electrical, x8 mechanical)
	 • One PCIe slot riser card (iPC **FCP1URISER2**), which supports:
	     o One LP/HL, single-width slot (x16 electrical, x16 mechanical)

Feature	Details

Riser Card Support (Cont.)	• Riser card (iPC **FCP1URISER2KIT**), which supports:
	   ○ One LP/HL, single-width slot (x16 electrical, x16 mechanical)
	   ○ One x8 PCIe MCIO connector with retimer
	
	PCIe* Interposer Riser Slot
	• Interposer riser card supports x8 PCIe lanes, routed from CPU 1 via Riser Slot #2
	• PCIe 5.0 support for 64 GB/s
	• PCIe Interposer Riser Slot supports the PCIe interposer riser card as an accessory option. This card supports one PCIe add-in card (x8 electrical, x8 mechanical). The PCIe interposer riser card can be used only when it is connected to the PCIe riser card in Riser Slot #2. The interposer riser card uses x8 PCIe data lanes routed from the PCIe MCIO connector on the PCIe riser card. The Intel® accessory kit (iPC FCP1URISER2KIT) includes the PCIe interposer riser card, PCIe riser card, and PCIe interposer cable.
	
	Riser Slot #3
	• Riser Slot #3 supports x16 PCIe lanes, routed from CPU 1
	• PCIe 5.0 support for up to 64 GB/s
	Riser Slot #3 supports the following Intel riser card options:
	• Two PCIe slot riser card (iPC **FCP2URISER3STD**), which supports:
	   ○ Two LP/HL single-width slots (x16 mechanical, x8 electrical)
	• NVMe riser card (iPC **CYPRISER3RTM**), which supports:
	   ○ Two PCIe NVMe* SlimSAS* connectors with retimers

PCIe* NVMe* Support	• Support for up to 18 PCIe NVMe Interconnects
	   ○ 16 onboard MCIO connectors, eight per processor
	   ○ Two M.2 NVMe/SATA connectors
	• Additional NVMe support through select riser card options (See Riser Card Support)

Video Support	• Integrated 2D video controller • 128 MB of DDR4 video memory • One DB-15 VGA Port in the back of the server board • One 2x7 VGA header on the front right side of the server board

Onboard SATA Support	• 10 x SATA III ports (6 Gb/s, 3 Gb/s, and 1.5 Gb/s transfer rates supported)
	   ○ Two M.2 connectors: SATA / PCIe
	   ○ Two 4-port Mini-SAS HD (SFF-8643) connectors

USB Support	• One USB 3.0 and two USB 2.0 connectors on the back edge of the board • Internal 26-pin connector for optional one USB 3.0 port and one USB 2.0 port front panel support
Serial Support	• One external RJ-45 Serial Port A connector on the back edge of the server board
Server Management	• Integrated Baseboard Management Controller (BMC) with support for OpenBMC • 1000BASE-T Ethernet port (RJ45) dedicated to server management • Integrated BMC Web Console • Intelligent Platform Management Interface (IPMI) 2.0 compliant • Support for Intel® Data Center Manager (Intel® DCM) • Support for Intel® Server Debug and Provisioning Tool (Intel® SDP Tool) • Redfish* compliant • Light Guided Diagnostics • Optional Advanced Server Management features (Purchased separately)
System Configuration and Recovery Jumpers	• BIOS load defaults • BIOS password clear • Intel® Management Engine firmware force update Jumper • BIOS_SVN downgrade • BMC_SVN downgrade

Feature	Details
Security Support	• Intel® Platform Firmware Resilience (Intel® PFR) technology with an I2C interface • Intel® Software Guard Extensions (Intel® SGX) • Converged Intel® Boot Guard and Trusted Execution Technology (Intel® TXT) • Intel® Total Memory Encryption – Multi-Key (Intel® TME-MK) • Trusted platform module 2.0 (China version) – iPC AXXTPMCHNE8 (accessory option) • Trusted platform module 2.0 (rest of the world) – iPC AXXTPMENC9 (accessory option)
BIOS	• Unified Extensible Firmware Interface (UEFI)-based BIOS (legacy boot not supported)

2.2 Server Board Component / Feature Identification
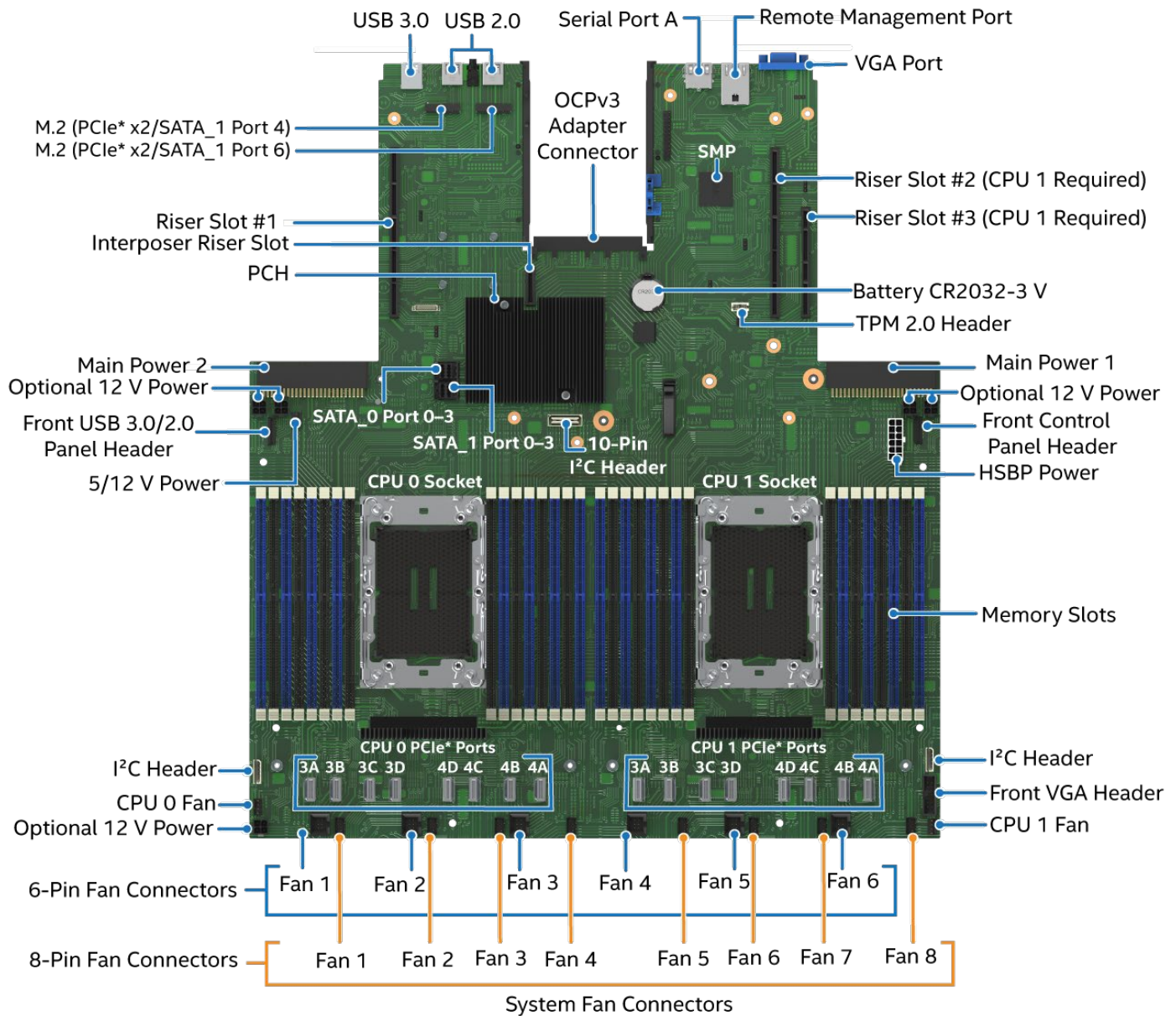
Figure 2. Intel® Server Board M50FCP2SBSTD Component / Feature Identification

Note: The features identified in Figure 2 represent their intended usage when the board is integrated into an Intel® chassis.

The server board includes LEDs to identify system status and/or indicate a component fault. The following figures identify Intel® Light Guided Diagnostic LEDs on the server board. For more information about the Intel® Light-Guided Diagnostics, see Chapter 11.
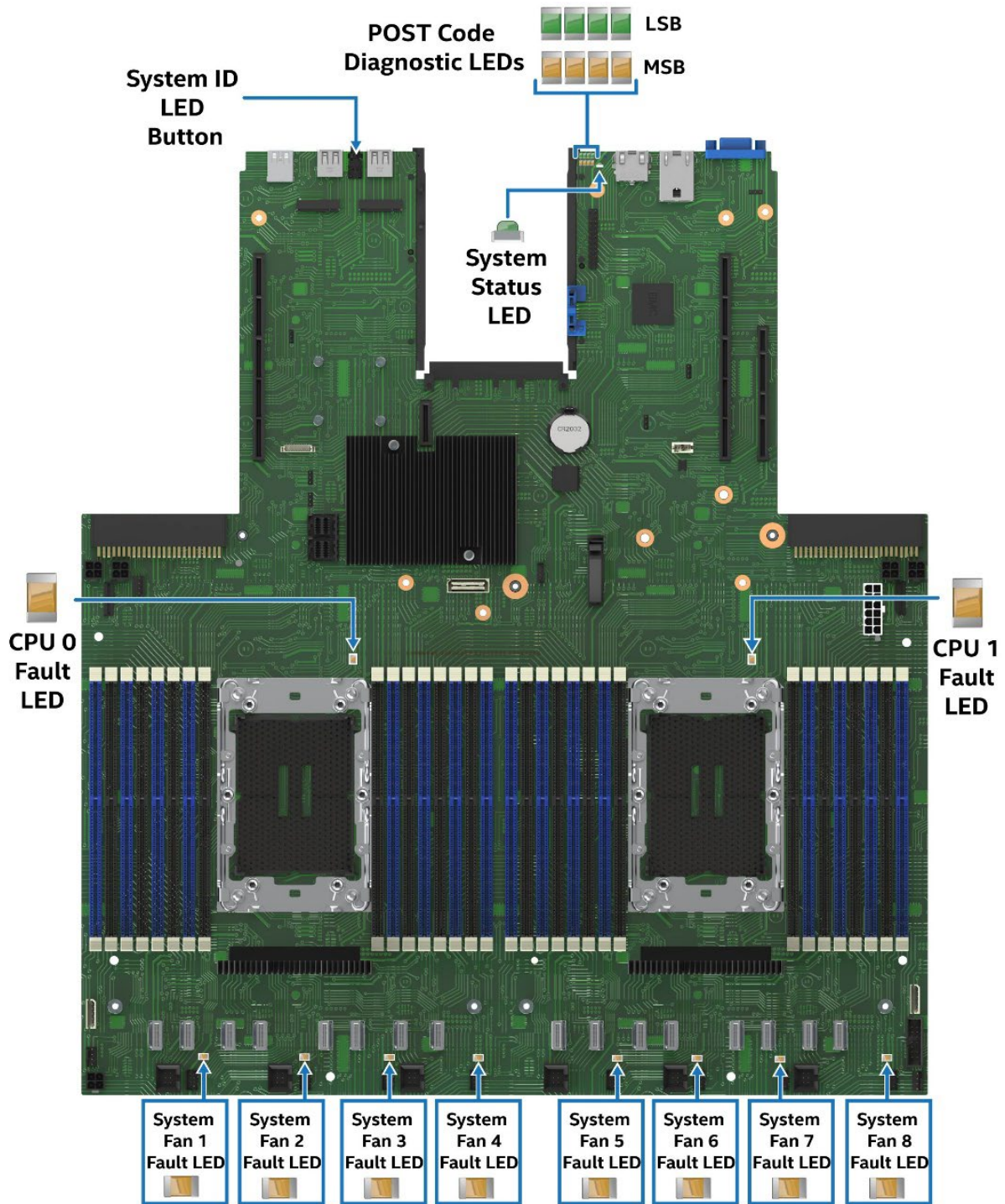
Figure 3. Intel® Light-Guided Diagnostics – LED Identification

Note: The system fan fault LEDS in Figure 3 are only for the 8-pin fan connectors.

21
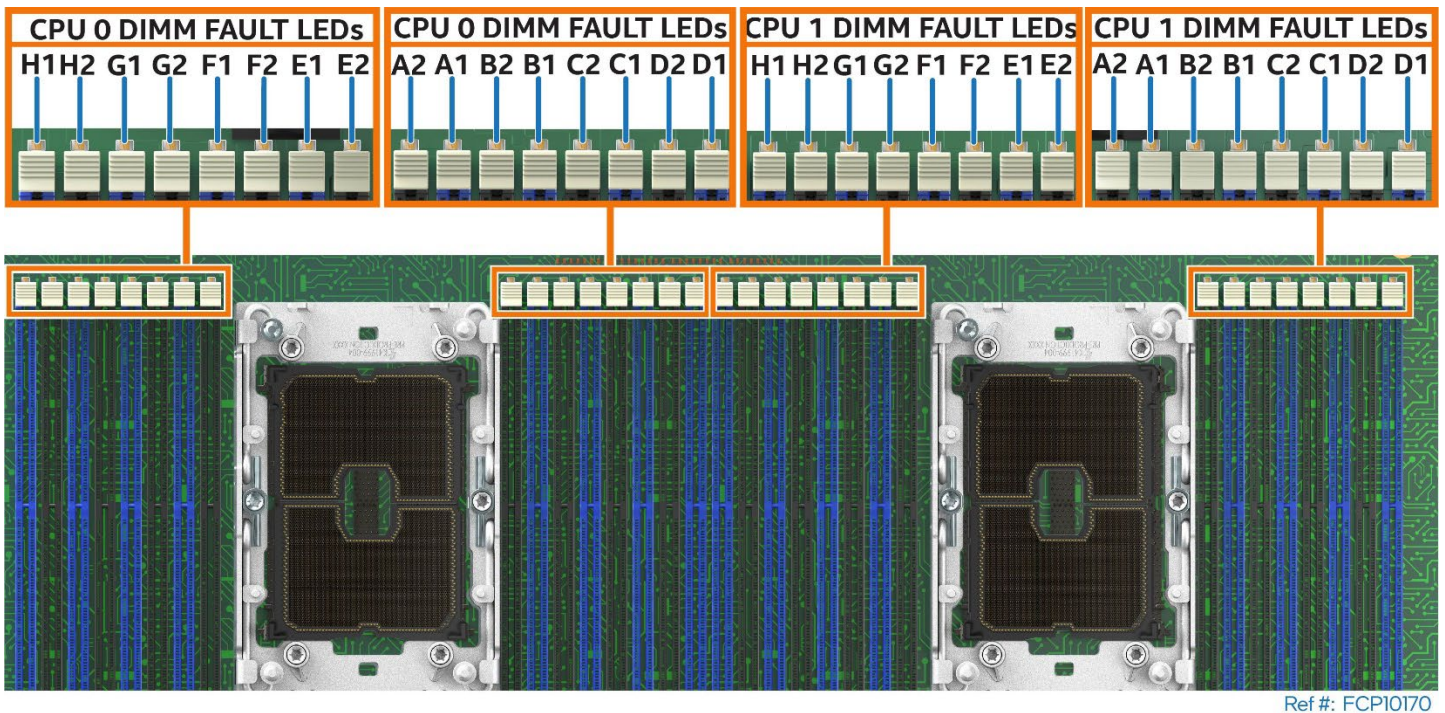
Ref #: FCP10170

Figure 4. Intel® Light-Guided Diagnostics – Memory Fault LEDs

The server board includes several jumper headers (see Figure 5) that can be used to configure, protect, or recover specific features of the server board. For more information about the jumpers, see Chapter 13.
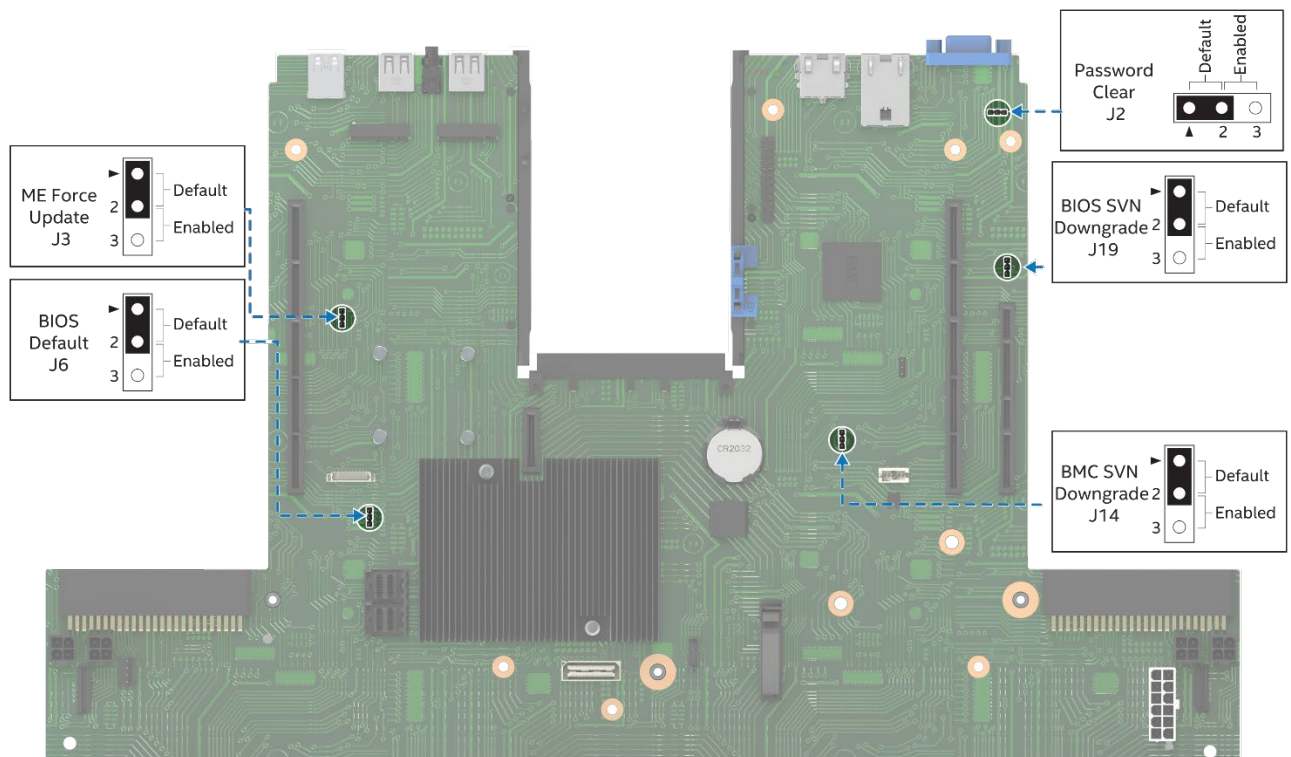
Ref #: FCP10374

Figure 5. System Configuration and Recovery Jumpers

2.3 Server Board Dimensions

The following figure shows the Intel® Server Board M50FCP2SBSTD dimensions.

18.9"
(480 mm)

16.9"
(428 mm)

Baseboard Thickness: 0.08" (1.93 mm)
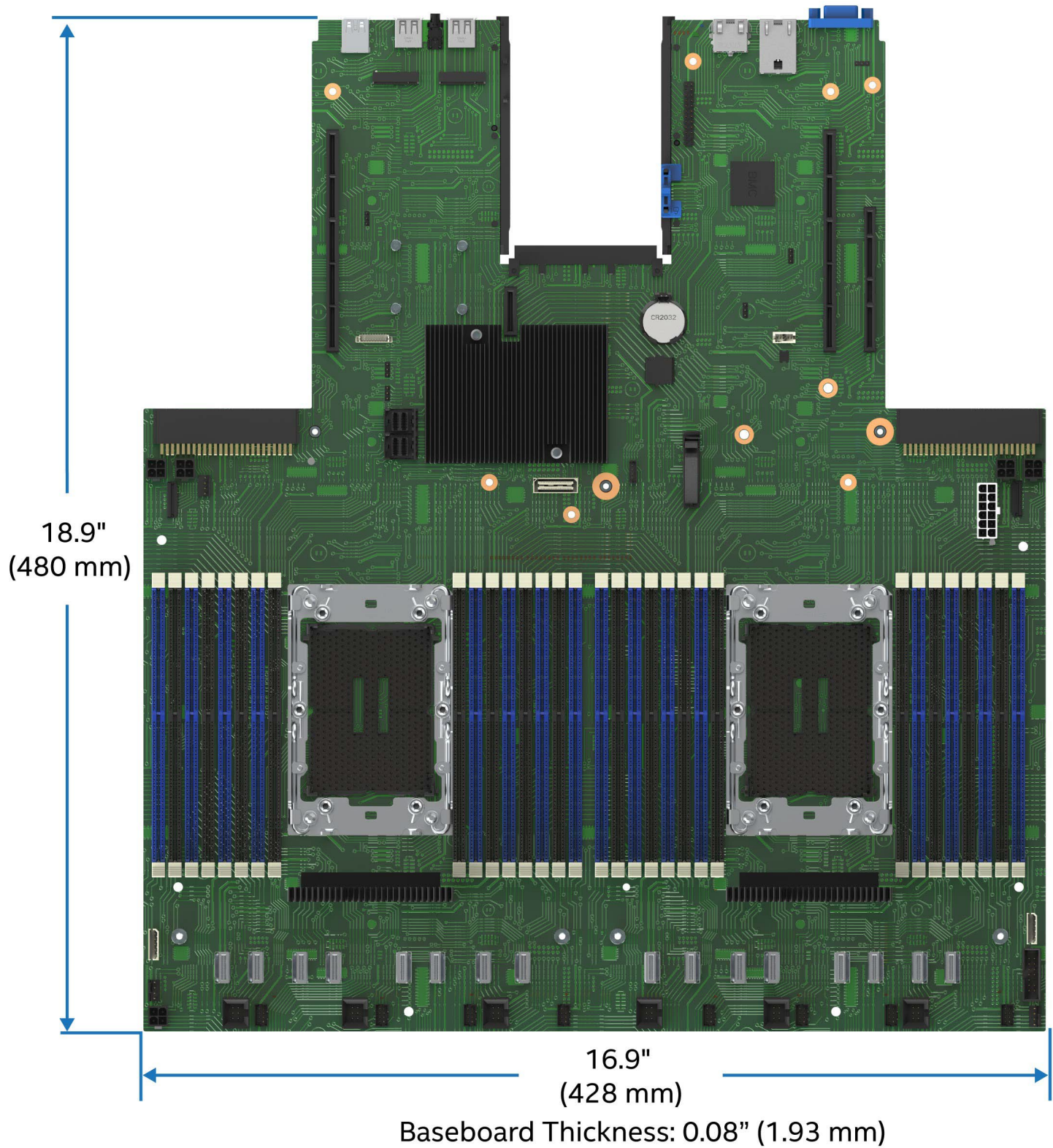
Ref #: FCP10291

Figure 6. Intel® Server Board M50FCP2SBSTD Board Dimensions

2.4   Server Board Mechanical Drawings

PLACEMENT KEEP OUT AREA HEIGHT=8MM

NO COMPONENT
PLACEMENT KEEP OUT AREA HEIGHT=0MM

PLACEMENT KEEP OUT AREA HEIGHT=8MM

PLACEMENT KEEP OUT AREA HEIGHT=8MM

PLACEMENT KEEP OUT AREA HEIGHT=4.32MM

PLACEMENT KEEP OUT AREA HEIGHT=2MM

PLACEMENT KEEP OUT AREA HEIGHT=10.45

PLACEMENT KEEP OUT AREA HEIGHT=9MM

PLACEMENT KEEP OUT AREA HEIGHT=8MM

PLACEMENT KEEP OUT AREA HEIGHT=10.45MM

PLACEMENT KEEP OUT AREA HEIGHT=1.5MM

PLACEMENT KEEP OUT AREA HEIGHT=2.2MM

PLACEMENT KEEP OUT AREA HEIGHT=8MM

PLACEMENT KEEP OUT AREA HEIGHT=5MM

NO COMPONENT
PLACEMENT KEEP OUT
AREA HEIGHT=0MM

PLACEMENT KEEP OUT AREA HEIGHT=2.2MM

PLACEMENT KEEP OUT AREA HEIGHT=3MM

NO COMPONENT
PLACEMENT KEEP OUT AREA HEIGHT=0MM

NO COMPONENT
PLACEMENT KEEP OUT AREA HEIGHT=0MM

PLACEMENT KEEP OUT
AREA HEIGHT=0MM

NO COMPONENT
PLACEMENT KEEP OUT AREA HEIGHT=0MM

KEEP OUT AREA HEIGHT=1MM

NO COMPONENT
PLACEMENT KEEP OUT AREA HEIGHT=0MM

NO COMPONENT
PLACEMENT KEEP OUT AREA HEIGHT=0MM

Ref #: FCP10330

Figure 7. Intel® Server Board M50FCP2SBSTD Top Surfaces Keep Out Zone (Drawing 1)
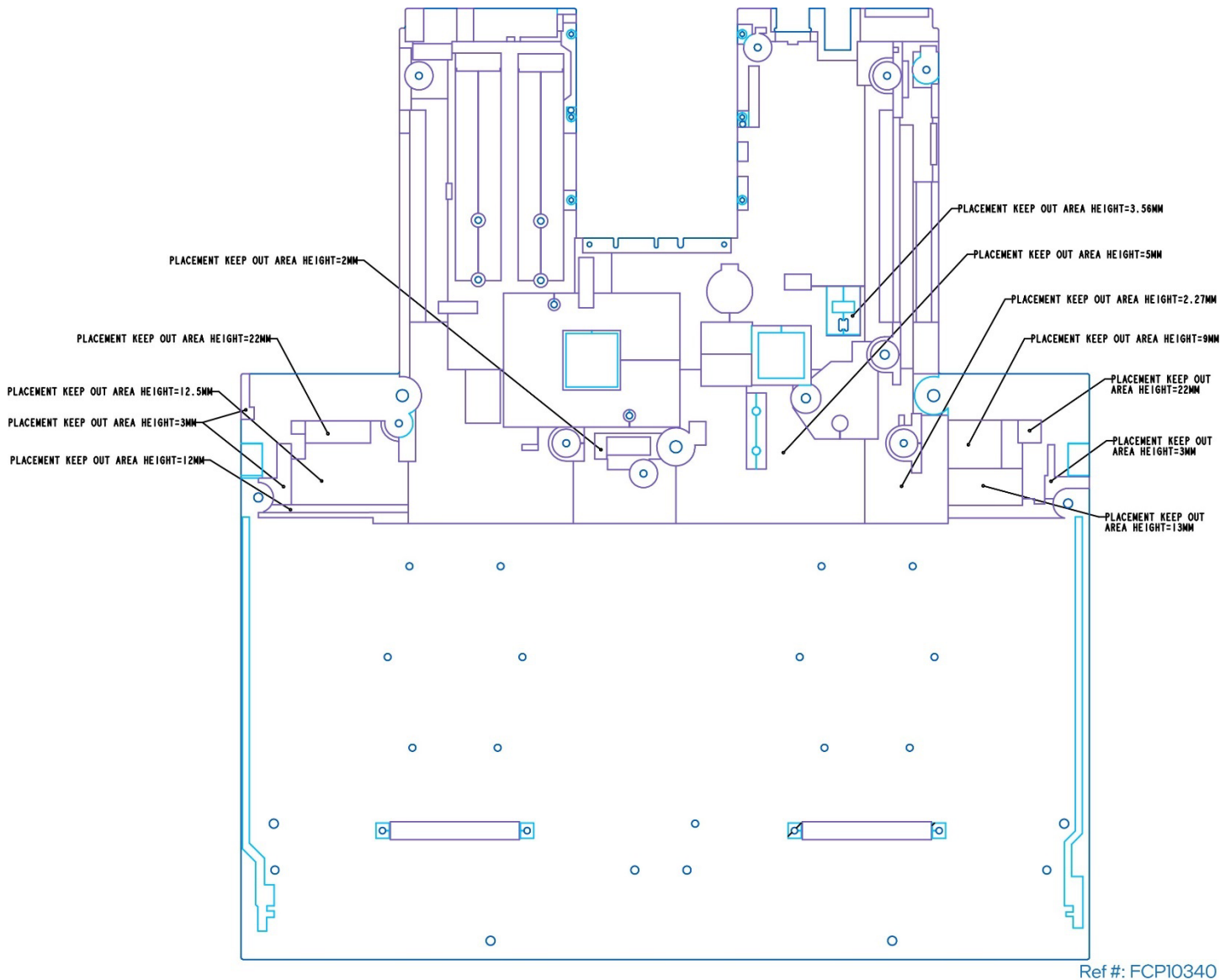
Figure 8. Intel® Server Board M50FCP2SBSTD Top Surface Keep Out Zone (Drawing 2)
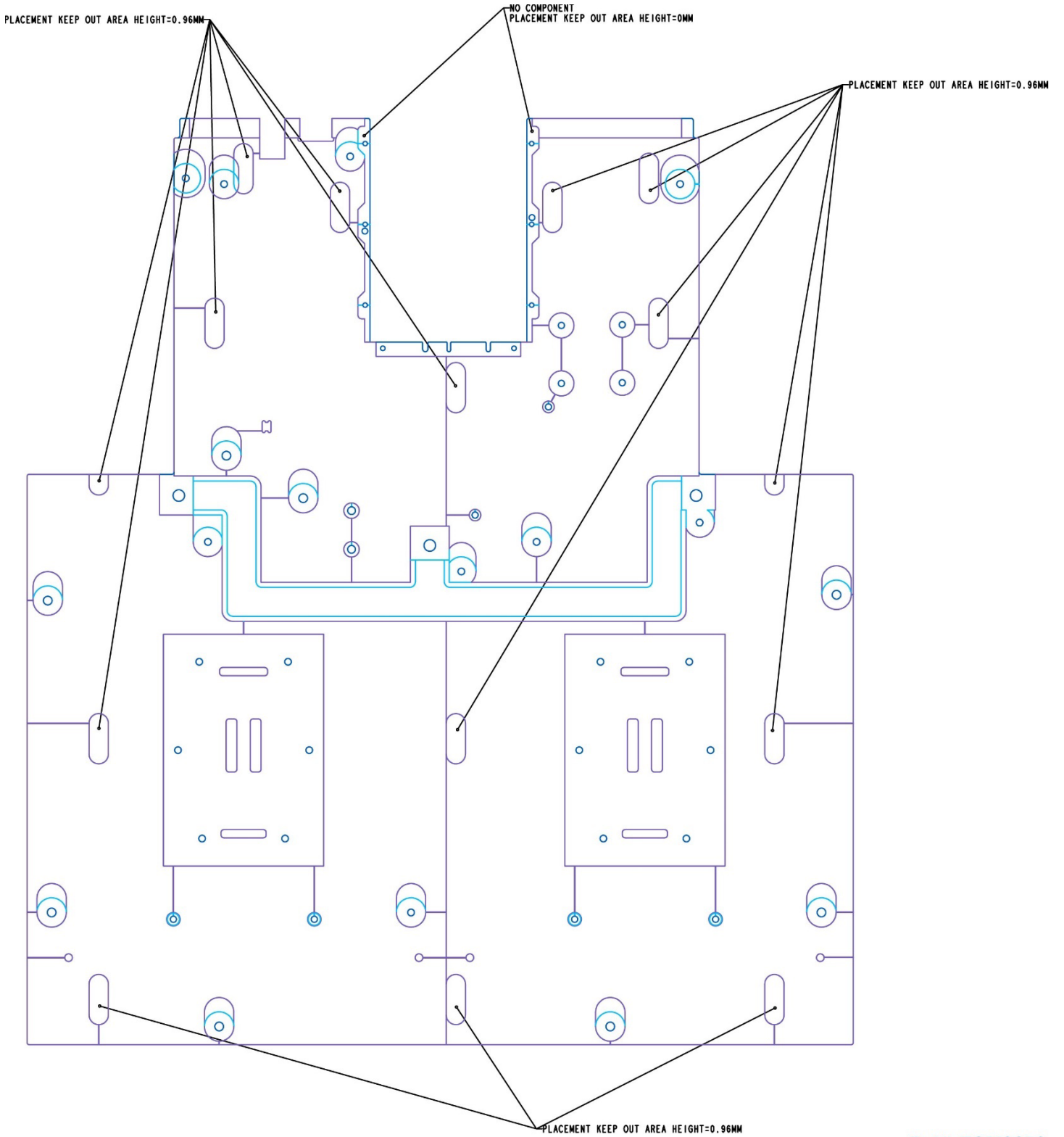
Figure 9. Intel® Server Board M50FCP2SBSTD Bottom Surface Keep Out Zone (Drawing 1)
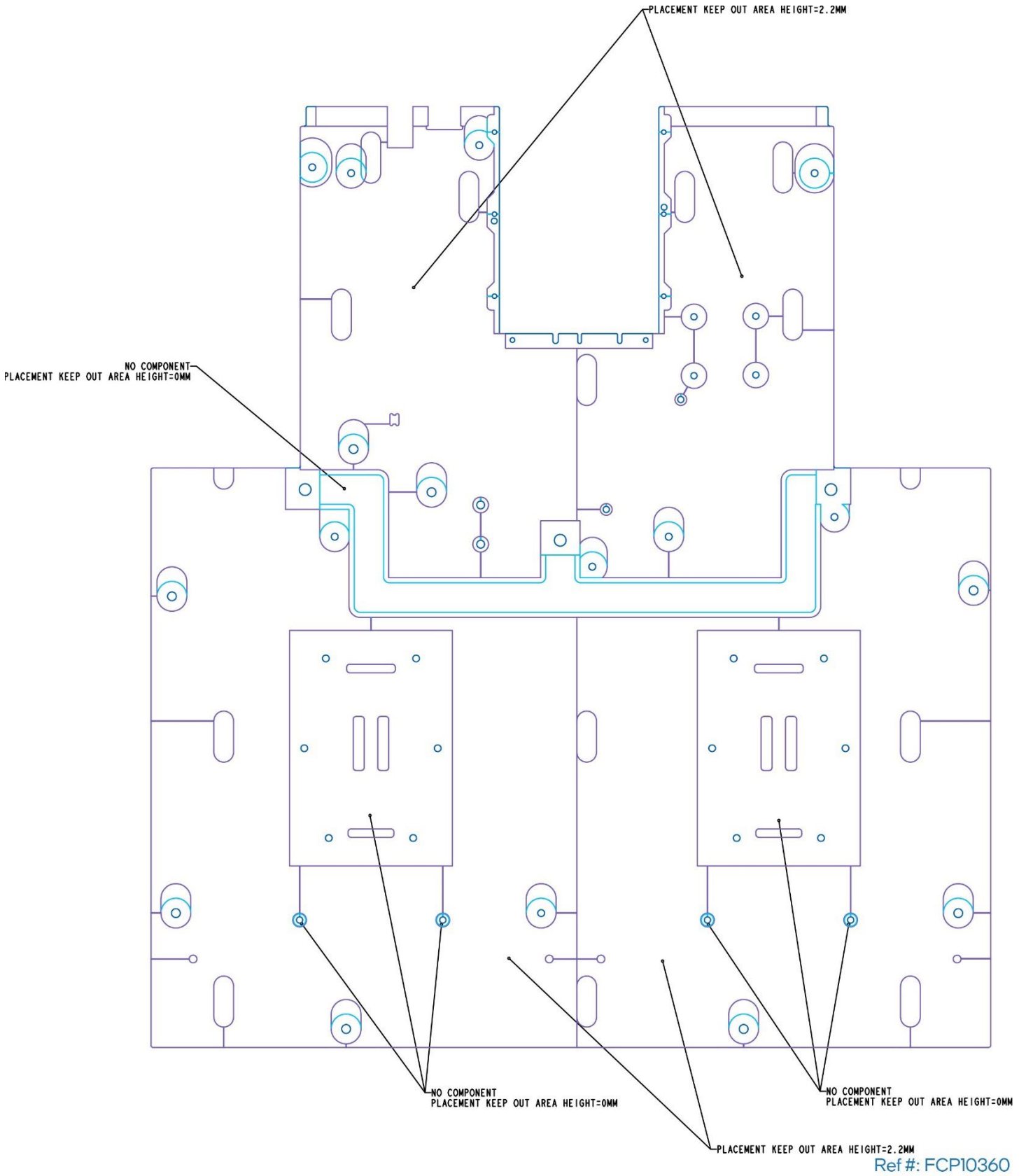
Figure 10. Intel® Server Board M50FCP2SBSTD Bottom Surface Keep Out Zone (Drawing 2)

Figure 11. Intel® Server Board M50FCP2SBSTD Components Position (Drawing 1)
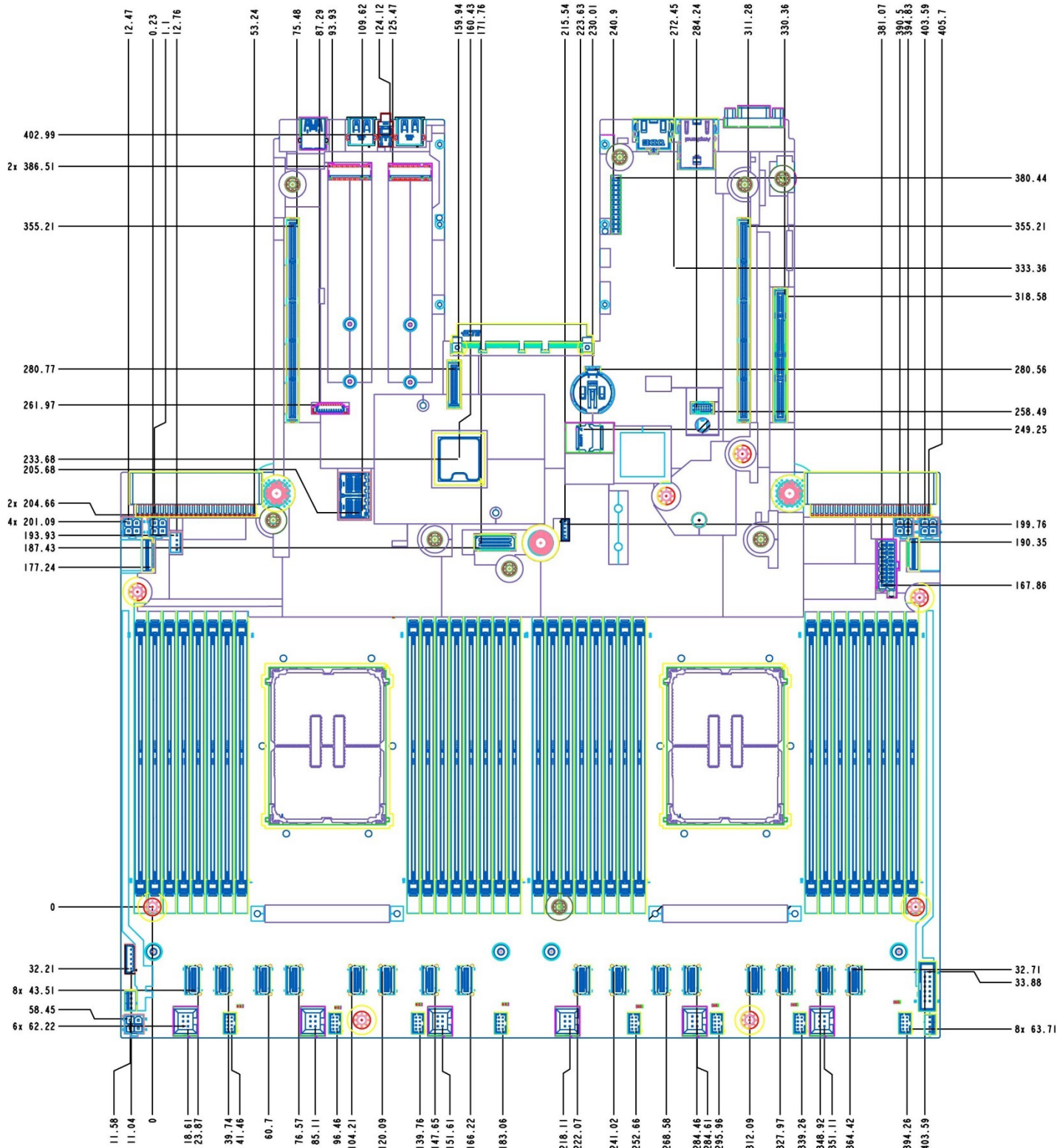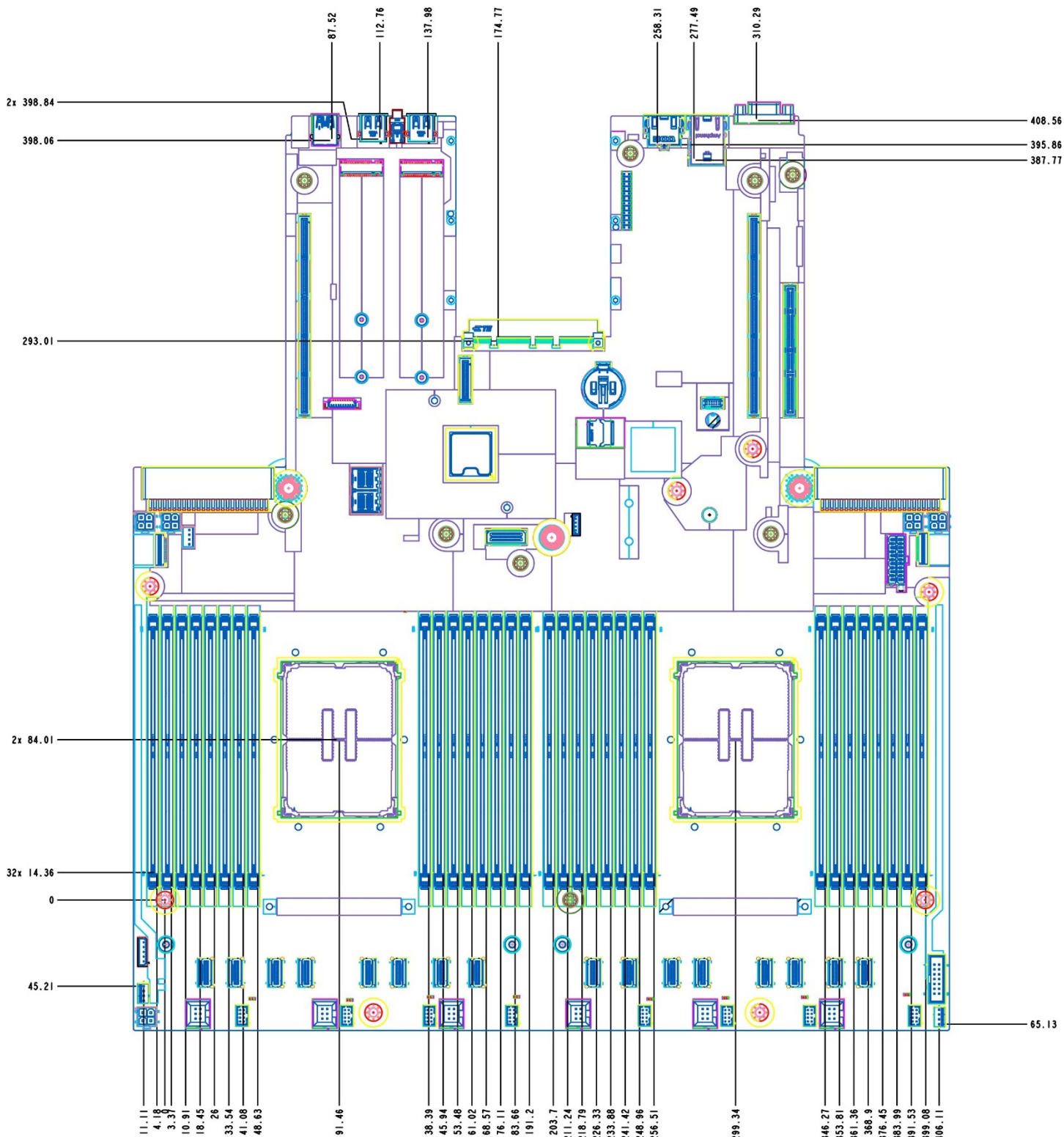
Ref #: FCP10310

Figure 12. Intel® Server Board M50FCP2SBSTD Components Position (Drawing 2)
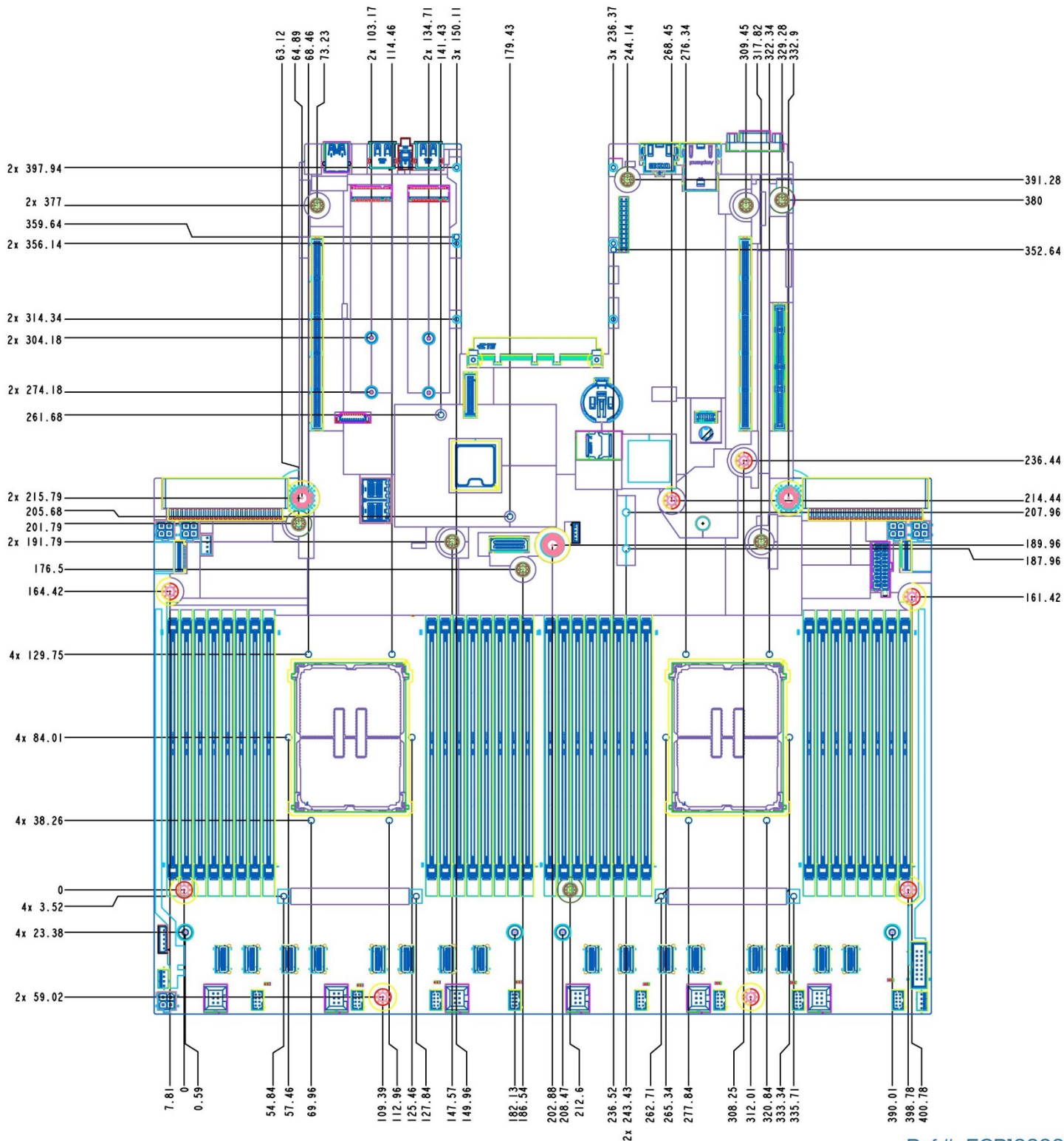
Ref #: FCP10320

Figure 13. Intel® Server Board M50FCP2SBSTD Holes Position

Ref #: FCP10300

2.5 Server Board Architecture Overview

The architecture of the Intel® Server Board M50FCP2SBSTD was developed around the integrated features and functions of the 4th Gen Intel® Xeon® Scalable processor family, Intel® C741 chipset PCH, and Aspeed AST2600* Server Management Processor (SMP).

The following figure provides an overview of the Intel® Server Board M50FCP2SBSTD architecture, showing the features and interconnects of the major subsystem components. Figure 2 provides a general overview of the physical server board, identifying key feature and component locations.
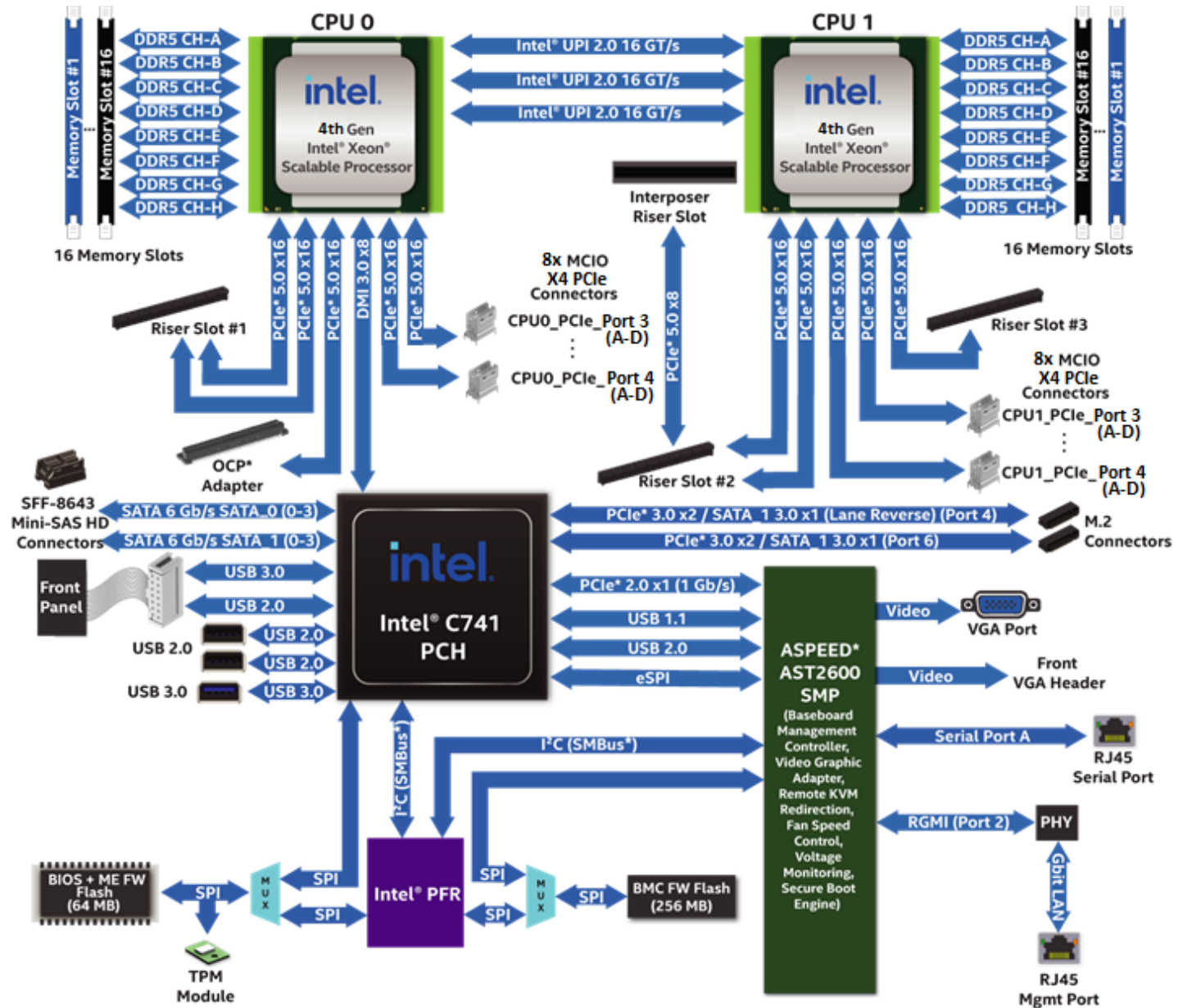
Figure 14. Intel® Server Board M50FCP2SBSTD Architectural Block Diagram

3. Processor Support

The server board includes two socket E LGA4677 processor sockets compatible with the 4th Gen Intel® Xeon® Scalable processors family.

Note: Previous generations of Intel® Xeon® processor and Intel® Xeon® Scalable processor families and their supported processor heat sinks are not compatible with the server board described in this document.

3.1 Processor Family Overview

Supported processor SKUs for this Intel® server product family can be identified as follows:

Intel® Xeon® Platinum **84**xxxx
Intel® Xeon® Gold **64**xxxx
Intel® Xeon® Gold **54**xxxx
Intel® Xeon® Silver **44**xxxx
Intel® Xeon® Bronze **34**xxxx

The following figure illustrates how to identify supported processor SKUs.
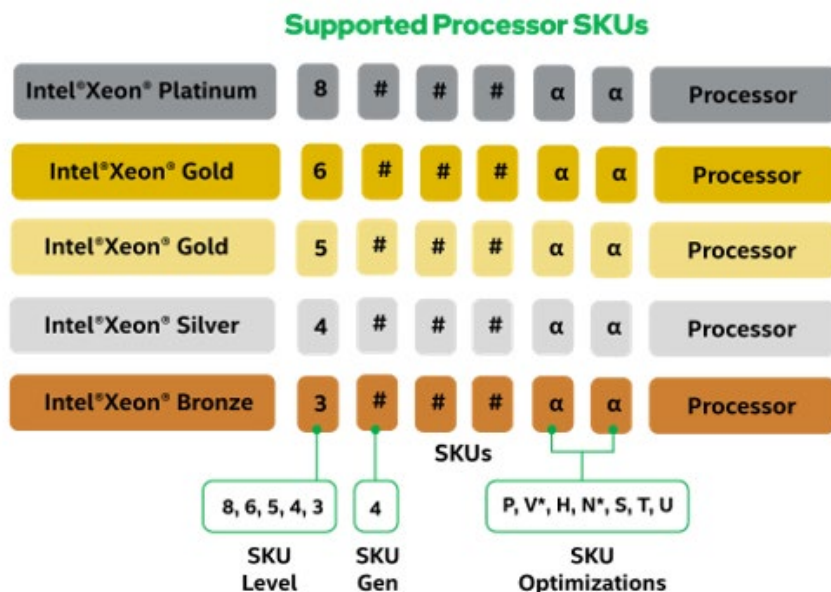
Figure 15. 4th Gen Intel® Xeon® Scalable Processor Identification

Notes:
- 4th Gen Intel® Xeon® Scalable processor SKU model numbers that end in (Q) are NOT supported.
- Intel® Xeon® Bronze processor SKUs are supported in single processor configurations only.

Table 3. 4ᵗʰ Gen Intel® Xeon® Scalable Processor Family Feature Comparison

Feature	Platinum 8xxx Processors	Gold 6xxx Processors	Gold 5xxx Processors	Silver 4xxx Processors
# of Intel® UPI Links	3	3	3	2
Intel® UPI Speed	16 GT/s	16 GT/s	16 GT/s	16 GT/s
Supported Topologies	2S-2UPI 2S-3UPI	2S-2UPI 2S-3UPI	2S-2UPI 2S-3UPI	2S-2UPI
Node Controller Support	No	No	No	No
RAS Capability	Advanced	Advanced	Advanced	Standard
Intel® Turbo Boost Technology	Yes	Yes	Yes	Yes
Intel® Hyper-Threading Technology (Intel® HT Technology)	Yes	Yes	Yes	Yes
Intel® Advanced Vector Extensions 512 (Intel® AVX-512) ISA Support	Yes	Yes	Yes	Yes
Intel® AVX-512 – # of 512b FMA Units	2	2	1	2
# of PCIe* Lanes	80	80	80	80
Intel® Volume Management Device (Intel® VMD)	Yes	Yes	Yes	Yes

Note: Features may vary between processor SKUs.

See the 4ᵗʰ Gen Intel® Xeon® Scalable processor specifications and product briefs for additional information.

3.1.1 Supported Technologies

The 4ᵗʰ Gen Intel® Xeon® Scalable processors combine several key system components into a single processor package including the processor cores, Integrated Memory Controllers (IMCs), and Integrated IO Module.

The core features and technologies for the processor family include:

- Intel® Ultra Path Interconnect (Intel® UPI): supports up to 16 GT/s
- Intel® Speed Shift Technology
- Intel® 64 architecture
- Enhanced Intel® SpeedStep® Technology
- Intel® Turbo Boost Technology 2.0
- Intel® Hyper-Threading Technology (Intel® HT Technology)
- Intel® Virtualization Technology (Intel® VT) for IA-32, Intel® 64 and Intel® Architecture (Intel® VT-x)
- Intel® Virtualization Technology (Intel® VT) for Directed I/O (Intel® VT-d)
- Execute Disable Bit
- Intel® Trusted Execution Technology (Intel® TXT)
- Intel® Advanced Vector Extensions (Intel® AVX-512)
- Intel® Advanced Encryption Standard New Instructions (Intel® AES-NI)
- Intel® Deep Learning Boost (Intel® DL Boost) through VNNI
- Intel® Speed Select Technology (Intel® SST) on select processor SKUs
- Intel® Resource Director Technology (Intel® RDT)

3.2 Processor Heat Sink Module (PHM) Overview

The server board includes two processor socket assemblies, each consisting of a processor socket and bolster plate. The factory installed bolster plate is secured to the server board and is generally used to align the processor cooling hardware over the processor socket and secure it to the server board.

Processor cooling options in a server system may use a passive or active heat sink that use airflow to dissipate heat generated by the processors. Other processor cooling options may use liquid cooling plates, where cool liquid is pumped through the cooling plates to absorb and evacuate the heat from the processor.

For air cooled systems. the processor and heat sink are generally pre-assembled into a single Processor Heat-sink Module (PHM) before being installed onto the processor socket assembly. The PHM concept reduces the risk of damaging pins within the processor socket during the processor installation process.

Note: The Intel® Server M50FCP Family only supports passive air-cooled options.

A PHM assembly consists of a processor, a processor carrier clip, and the processor heat sink. The following figure identifies each component associated with the PHM and processor socket assembly.
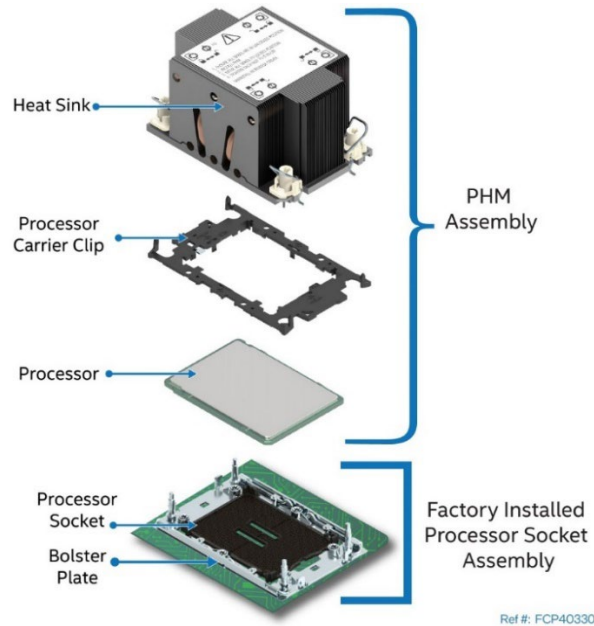
Figure 16. PHM Components and Processor Socket Reference Diagram

Note: Figure 16 is intended as a general reference to components that make up the PHM and processor socket assemblies. The components shown may or may not match exactly what may be used. The diagram does NOT define the process necessary to assemble the PHM or install it onto the processor socket. See Appendix H for recommended assembly and installation instructions.

3.2.1 Processor Carrier Clips

There are two types of processor carrier clips supported by the 4th Gen Intel® Xeon® Scalable processor family for this server product family, they are identified as "E1A" and "E1B".

E1A Processor Carrier Clip   E1B Processor Carrier Clip
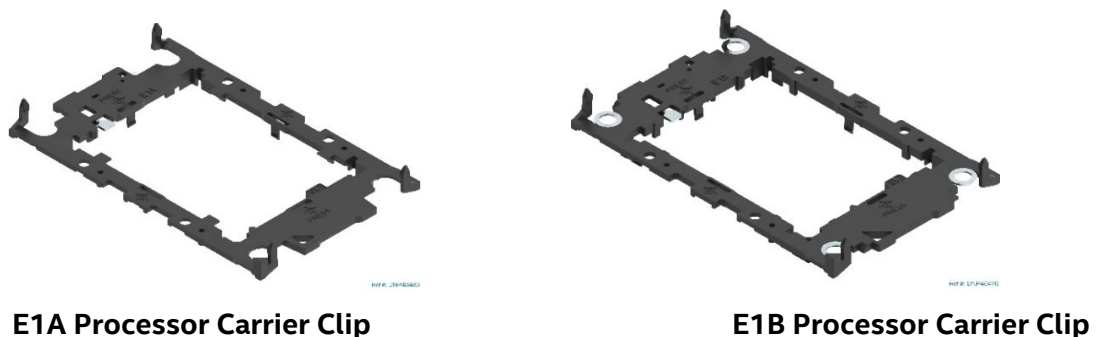
Figure 17. Supported Processor Carrier Clips

Each type of processor carrier clip will include identifier markings as shown in Figure 18.

The selected processor SKU determines which processor clip to use when assembling the processor heat sink module (PHM). A processor carrier clip identifier marking will be etched onto the processor heat spreader as shown in Figure 18.
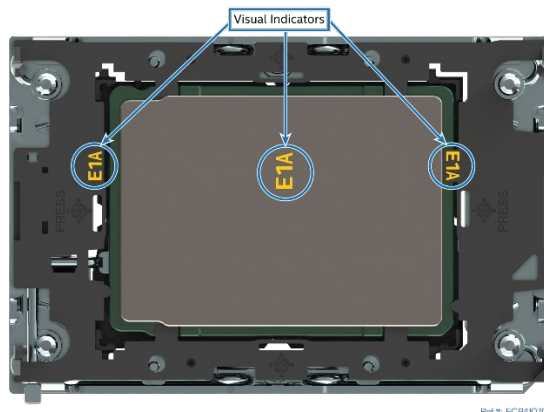
Figure 18. Processor Carrier Clip Identifier Markings

Note: The etched identifier location in the figure above is for illustration purposes only. The actual location and color may be different on the actual processor and carrier clip.

3.2.2   Processor Cooling Requirements

For the server system to support optimal operation and long-term reliability, the thermal management solution of the selected server chassis must dissipate enough heat generated from within the chassis to keep the processors and other system components within their specified thermal limits.

For optimal operation and long-term reliability, processors in the 4th Gen Intel® Xeon® Scalable processor family must operate within their defined minimum and maximum case temperature (T_{CASE}) limits. See the 4th Gen *Intel® Xeon® Processor Scalable Family Thermal Mechanical Specifications and Design Guide* for additional information concerning processor thermal limits.

Note: It is the responsibility of the system and components architects to ensure compliance with the processor thermal specifications. Compromising processor thermal requirements impacts the processor performance and reliability.

Disclaimer: Intel® server boards contain and support several high-density VLSI and power delivery components that need adequate airflow to cool and remain within their thermal operating limits. Intel ensures through its own chassis development and testing that when an Intel server board and Intel chassis are used together, the fully integrated system meets the thermal requirements of these components. It is the responsibility of the system architect or system integrator who chooses to develop their own server system using an Intel server board and a non-Intel chassis, to consult relevant specifications and datasheets to determine thermal operating limits and necessary airflow to support intended system configurations and workloads when the system is operating within target ambient temperature limits. It is also their responsibility to perform adequate environmental validation testing to ensure reliable system operation. Intel cannot be held responsible if components fail or the server board does not operate correctly when published operating and non-operating limits are exceeded.

3.3 Processor Thermal Design Power (TDP)

The Intel® Server Board M50FCP2SBSTD supports the 4th Gen Intel® Xeon® Scalable processor family with a maximum thermal design power (TDP) limit of 350 W.

Note: The maximum supported processor TDP at the system level may be lower than what the server board can support. Supported power, thermal, and configuration limits of the chosen server chassis / system need to be considered to determine if the system can support the maximum processor TDP limit of the server board or not. Refer to the chosen server chassis/system documentation for additional processor support guidance.

3.4 Processor Population Rules

Note: The server board may support dual-processor configurations consisting of different processors that meet the following defined criteria. However, Intel does not perform validation testing of this configuration. In addition, Intel does not ensure that a server system configured with unmatched processors operates reliably. The system BIOS attempts to operate with processors that are not matched but are generally compatible. For optimal system performance in dual-processor configurations, Intel recommends that identical processors be installed.

When using a single processor configuration, the processor must be installed in the processor socket labeled "CPU_0".

Note: Some server board features may not be functional unless a second processor is installed. For the Intel® Server Board M50FCP2SBSTD, see Figure 14.

When two processors are installed, the following population rules apply:

- Both processors must have identical extended family, extended model number and processor type

Also:

- Both processors must have the same number of cores
- Both processors must have the same cache sizes for all levels of processor cache memory
- Both processors must support identical DDR5 memory frequencies

Note: Processors with different steppings can be mixed in a system if the rules mentioned in the above bullets are met.

Population rules are applicable to any combination of processors in the 4th Gen Intel® Xeon® Scalable processor family.

4. Memory Support

This chapter describes the architecture that drives the memory subsystem, supported memory types, memory population rules, and supported memory RAS features.

4.1 Supported Memory

The server board supports SDRAM DDR5 RDIMMs (standard RDIMMs, 3DS-RDIMMs, and 9x4 RDIMMs) and Intel® Optane™ persistent memory (PMem) 300 series modules. The server board may be populated with a combination of both DDR5 RDIMMs and Intel® Optane™ PMem 300 series modules.

Notes:
- Previous generation Intel® Optane™ persistent memory modules and previous generation DDR DIMMs are not supported.
- In this document, DDR5 DIMM and Intel® Optane™ PMem devices are commonly referred to as "memory module".

DDR5 is the next generation of double data rate synchronous dynamic random-access memory. DDR5 provides high data transfer rates, low power consumption, and increased bandwidth. Reduced working voltage of 1.1 V leads to better energy efficiency.

Intel® Optane™ persistent memory (Intel® Optane™ PMem) is an innovative technology that delivers a unique combination of affordable large memory capacity and data persistence (non-volatility). It represents a new class of memory and storage technology architected specifically for data center usage. The Intel® Optane™ PMem 300 series modules enable higher density (capacity per memory module) DDR5-compatible memory modules. Intel® Optane™ PMem 300 series has near-DRAM performance and advanced features not found in standard SDRAM. Intel® Optane™ PMem allows users to better optimize workloads by moving and maintaining larger amounts of data closer to the processor. Users can directly store and access data through Intel® Optane™ PMem instead of system storage, which minimizes latency. The persistent memory technology can help boost the performance of data-intensive applications, such as in-memory analytics, databases, content delivery networks, and high-performance computing (HPC). In addition, persistent memory technology delivers consistent service levels at scale with higher virtual machine and container density.

4.1.1 Standard DDR5 DIMM Support

The following figure shows a standard DDR5 DIMM.
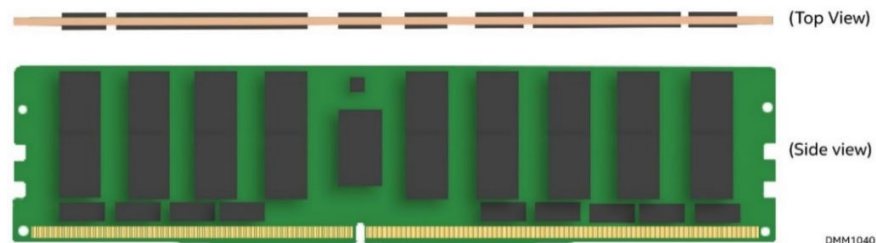
Figure 19. Standard SDRAM DDR5 DIMM

The server board supports DDR5 DIMMs with the following attributes:

- Registered DDR5 DIMM (standard RDIMM, 3DS-RDIMM, and 9x4 RDIMM)
  Note: 3DS = 3-dimensional stacking.
- All DDR5 RDIMMs must support ECC

- RDIMMs with thermal sensor on DIMM (TSOD)
- RDIMM speeds of up to 4800 MT/s
- RDIMM capacities of 8 GB, 16 GB, 32 GB, 64 GB, 128 GB, and 256 GB
- RDIMMs organized as Single Rank (SR), Dual Rank (DR)
- 3DS-RDIMM organized as Quad Rank (QR), or Oct Rank (OR)

The following tables list the DDR5 DIMM support guidelines.

Table 4. Supported DDR5 DIMM Memory

Type	Ranks[2] per DIMM and Data Width	DIMM Capacity (GB) (16 Gb DDR5 Density)	Maximum Speed (MT/s) at 1.1 V	
			1 DPC	2 DPC
RDIMM	SRx8	16	4800[1]	4400[1]
	SRx4	32		
	SRx4 9x4	32		
	DRx8	32		
	DRx4	64		
	DRx4 9x4	64		
3DS–RDIMM	(QR/OR)x4	128 (2H) 256 (2H)		

Notes: (1) Refer to the DIMM datasheets for more information. (2) SR = Single Rank, DR = Dual Rank, QR = Quad Rank, OR = Oct Rank

Table 5. Maximum Supported Standard SDRAM DIMM Speeds by Processor Shelf

Processor Family	Maximum DIMM Speed (MT/s) by Processor Shelf			
	Platinum 8xxx Processors	Gold 6xxx Processors	Gold 5xxx Processors	Silver 4xxx Processors
4th Gen Intel® Xeon® Scalable processor family	4800 at 1DPC, 4400 at 2DPC	4800 at 1DPC, 4400 at 2DPC	4400 at 1DPC, 4400 at 2DPC	4000 at 1DPC, 4000 at 2DPC

Note: Specifications apply only to memory chips mounted by surface mounted technology (SMT) method. Refer to the DIMM datasheets for more information.

4.1.2 Intel® Optane™ PMem 300 Series Module Support

The Intel® Server Board M50FCP2SBSTD supports Intel® Optane™ persistent memory (PMem) 300 series modules. The following figure shows an Intel® Optane™ PMem 300 series module.
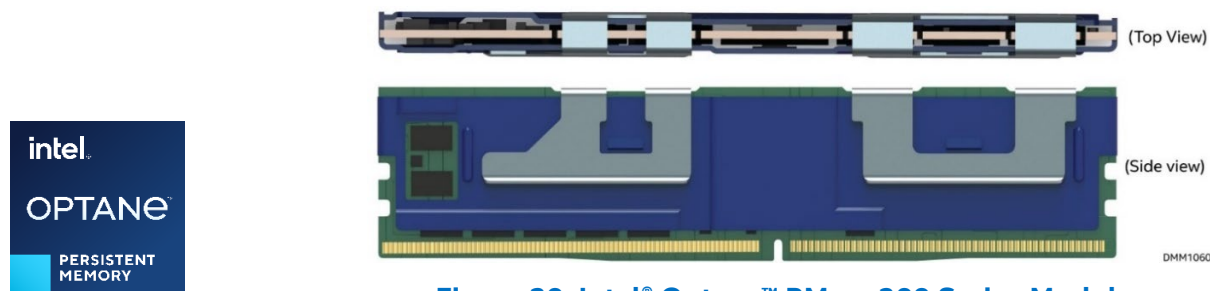
Figure 20. Intel® Optane™ PMem 300 Series Module

The Intel® Optane™ PMem 300 series supports the following attributes:

- Always-enabled AES-256 encryption
- Cache coherent: like DRAM, contains evicted information from the Last Level Cache (LLC)

- Byte-addressable memory
- Higher endurance than enterprise class SSDs

The following operating mode is supported:

- App Direct (AD) mode

See Section 4.5 for memory RAS features and Intel® Optane™ PMem 300 series compatibility with security features Intel® Software Guard Extensions (Intel® SGX) and Intel® Total Memory Encryption – Multi-Key (Intel® TME-MK).

4.1.2.1 Intel® Optane™ PMem 300 Series Module: App Direct Mode

In App Direct mode, applications and the operating system are explicitly aware that there are two types of direct load/store memory in the platform. They can direct which type of data read or write is suitable for DRAM or Intel® Optane™ PMem 300 series modules. Operations that require the lowest latency and do not need permanent data storage can be executed on DRAM DIMM, such as database "scratch pads".

Data that needs to be made persistent or structures that are very large can be routed to the Intel® Optane™ persistent memory. The App Direct mode must be used to make data persistent in memory. This mode requires an operating system or virtualization environment enabled with a persistent memory-aware file system.

App Direct mode requires both driver and explicit software support. To ensure operating system compatibility, visit https://www.intel.com/content/www/us/en/products/details/memory-storage/optane-dc-persistent-memory.html

4.1.2.2 Intel® Optane™ PMem configuration using the BIOS Setup Utility

Following the installation of Intel® Optane™ PMem devices into the system, they need to be configured using the <F2> BIOS setup utility. After powering up the system press <F2> on the keyboard to access the utility. From the main BIOS Setup page, navigate to Advanced > PCI Configuration > UEFI Option ROM Control > Intel® Optane™ Persistent Memory Configuration. The main Intel® Optane™ PMem Configuration screen provides links to the various device information and setup screens (see figure below). Refer to the *Intel® Optane™ Persistent Memory Start Up Guide* for details on how to configure Intel® Optane™ PMem.
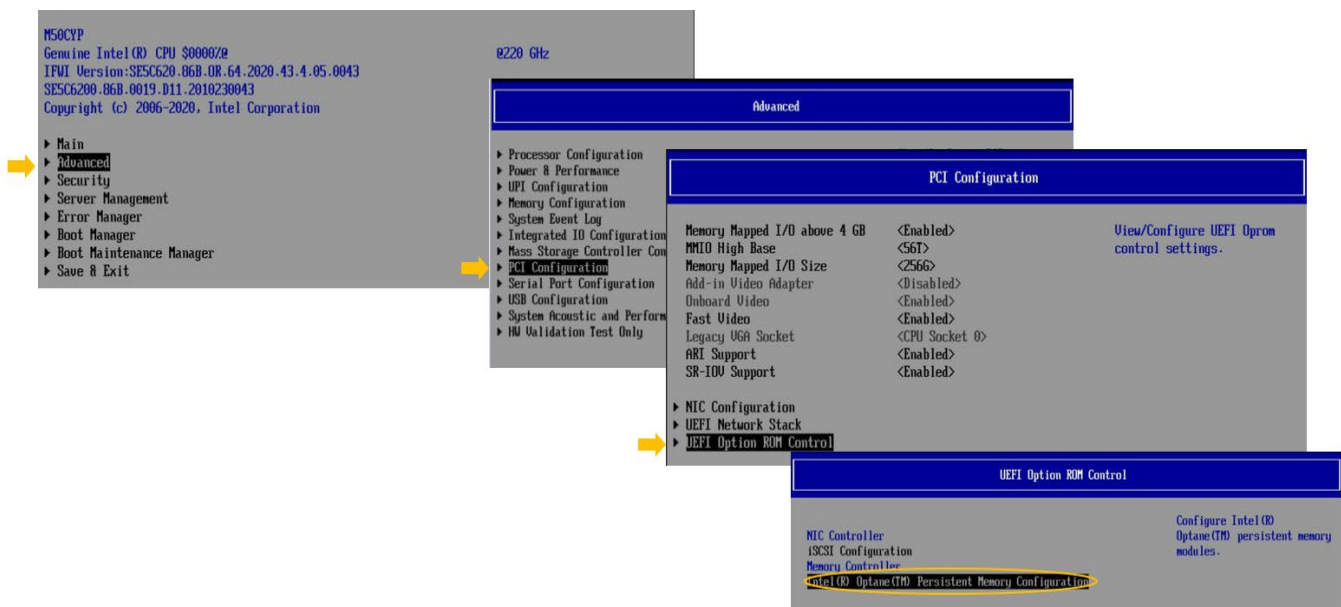
Figure 21. <F2> BIOS Setup Utility Screens Navigation for Intel® Optane™ PMem Setup Options

The main Intel® Optane™ PMem Configuration screen provides links to the various device information and setup screens.
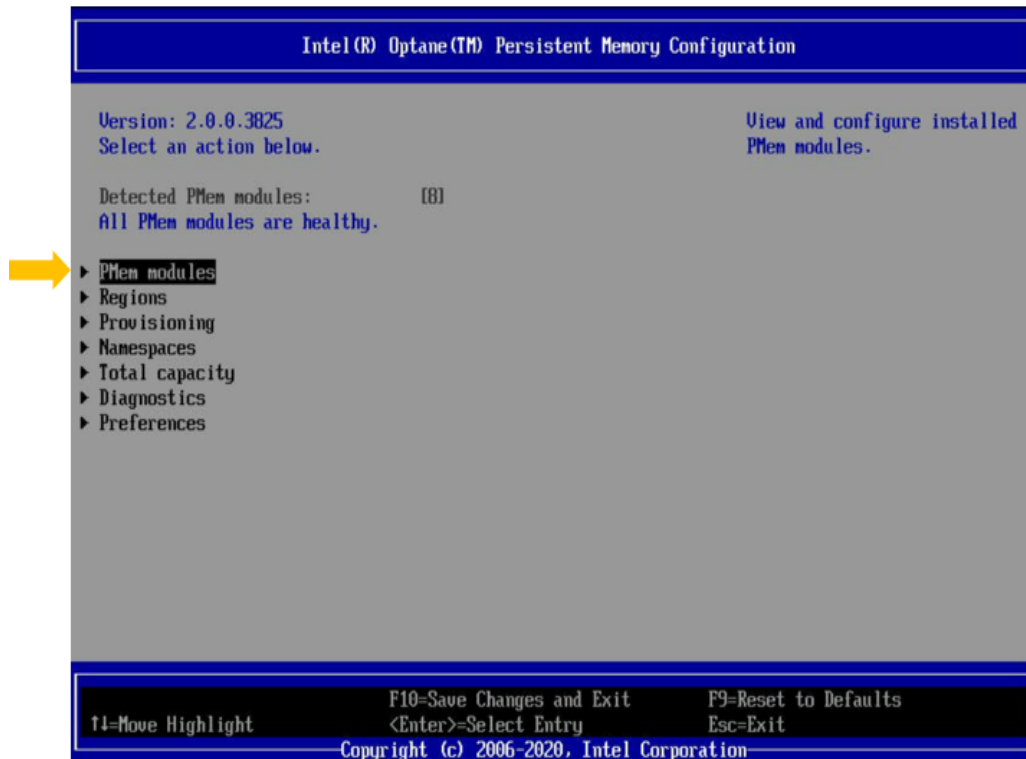
Figure 22. Intel® Optane™ PMem Configuration Menu in <F2> BIOS Setup Utility

4.2 Memory Subsystem Architecture

The server board has 32 memory slots, 16 slots per processor, as shown in the following figure.
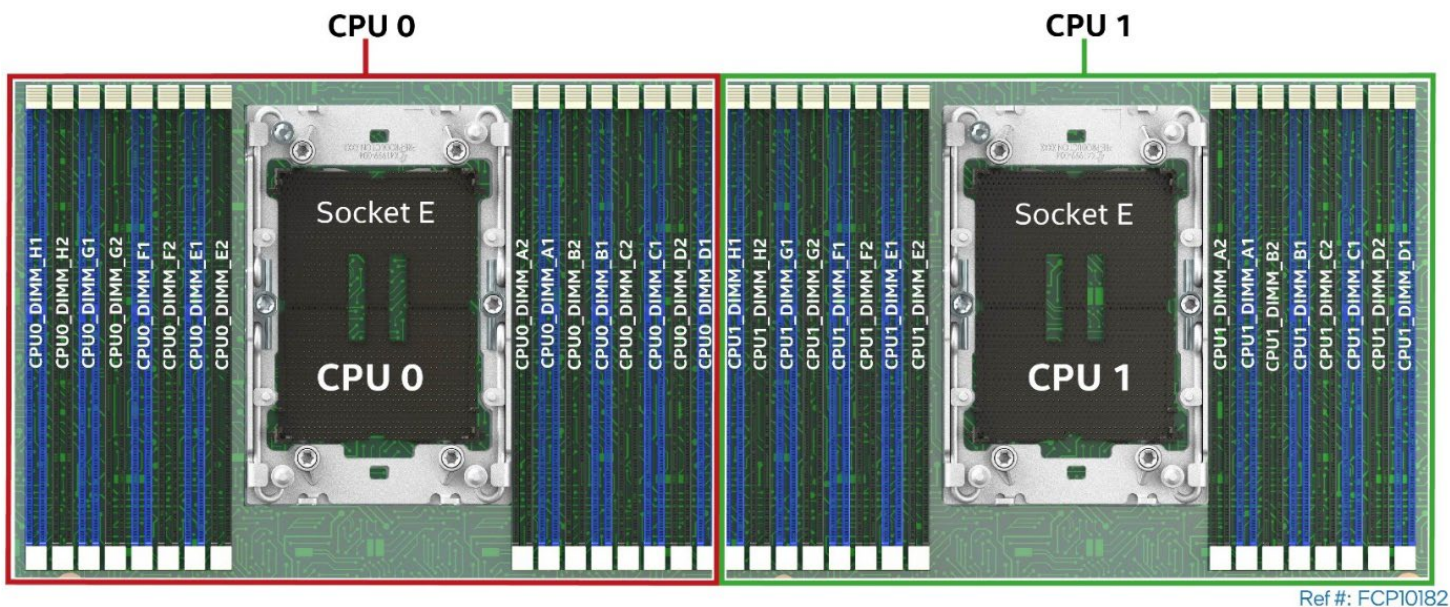
Figure 23. Server Board Memory Slot Layout

Each processor has four Integrated Memory Controllers (IMCs), each supporting two memory channels (see the following figure). Memory channels are identified A-H. Each memory channel supports two memory slots—slot 1 (blue slot) and slot 2 (black slot).
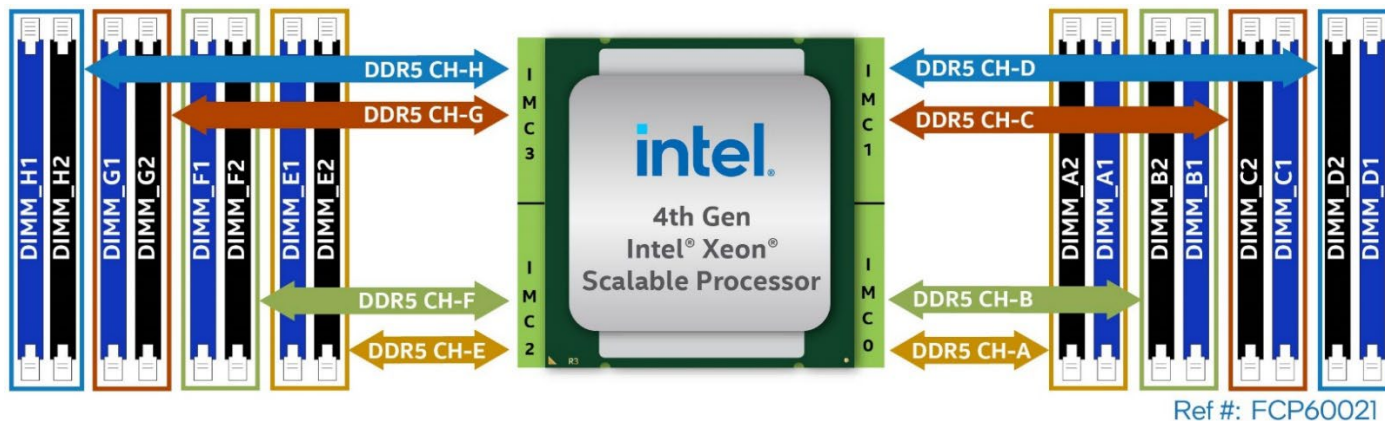
Figure 24. Memory Slot Connectivity

4.3   Intel DDR5 DIMM Support Disclaimer

Intel validates and only supports system configurations where all installed DDR5 DIMMs have matching "Identical" or "Like" attributes (see the following table). A system configured with DDR5 DIMMs from different vendors is supported by Intel if all other DDR5 "Like" DIMM attributes match.

Intel does not perform system validation testing nor will it support system configurations where all populated DDR5 DIMMs do not have matching "Like" DIMM attributes as listed in the following table

Intel only supports Intel server systems configured with DDR5 DIMMs that have been validated by Intel and are listed on Intel's Tested Memory list for the given Intel server product family.

Intel may offer and ship pre-integrated fully configured server systems. All DDR5 DIMMs within a given server system as shipped by Intel are identical. All installed DIMMs have matching attributes as listed in the *"Identical" DDR5 DIMM Attributes* column in the following table.

When purchasing multiple fully integrated server systems with the same configuration from Intel, Intel reserves the right to use "Like" DIMMs between server systems. At a minimum, "Like" DIMMS will have matching DIMM attributes as listed in the following table. However, the DIMM model #, revision #, or vendor may be different.

For warranty replacement, Intel will make every effort to ship back an exact match to the one returned. However, Intel may ship back a validated "Like" DIMM. A "Like" DIMM may be from the same vendor but may not be the same revision # or model #, or it may be an Intel-validated DIMM from a different vendor. At a minimum, all "Like" DIMMs shipped from Intel will match attributes of the original part according to the definition of "Like" DIMMs in the following table.

Table 6. DDR5 DIMM Attributes Table for "Identical" and Like DIMMs

• DDR5 DIMMs are considered "Identical" when ALL listed attributes between the DIMMs match • Two or more DDR5 DIMMs are considered "Like" DIMMs when all attributes minus the Vendor, and/or DIMM Part # and/or DIMM Revision#, are the same.			
Attribute	"Identical" DDR5 DIMM Attributes	"Like" DDR5 DIMM Attributes	Possible DDR5 Attribute Values
Vendor	Match	May be Different	Memory Vendor Name
DIMM Part #	Match	May be Different	Memory Vendor Part #
DIMM Revision #	Match	May be Different	Memory Vendor Part Revision #
SDRAM Type	Match	Match	DDR5
DIMM Type	Match	Match	RDIMM, 9x4 RDIMM
Speed (MT/s)	Match	Match	4000, 4400, 4800
Voltage	Match	Match	1.1 V

- DDR5 DIMMs are considered "Identical" when ALL listed attributes between the DIMMs match
- Two or more DDR5 DIMMs are considered "Like" DIMMs when all attributes minus the Vendor, and/or DIMM Part # and/or DIMM Revision#, are the same.

Attribute	"Identical" DDR5 DIMM Attributes	"Like" DDR5 DIMM Attributes	Possible DDR5 Attribute Values
DIMM Size (GB)	Match	Match	16 GB, 32 GB, 64 GB, 128 GB, 256 GB
Organization	Match	Match	2Gx80; 4Gx80; 8Gx80; 16Gx80; 32Gx80
DIMM Rank	Match	Match	1R, 2R, 4R, 8R
DIMM Raw Card (RC)	Match	Match	RC A, RC B, RC C, RC D, RC E, RC F
DRAM Width	Match	Match	x4, x8
DRAM Density	Match	Match	16 Gb

4.4 Memory Population

Note: The server board may support and operate with mixed memory configurations if the following population rules are followed. However**,** Intel will only provide support for mixed DDR5 DRAM DIMM configurations as defined in the Intel® DDR5 Support Disclaimer in Section 4.3.

The following memory population rules apply when installing DDR5 DIMMs:

- Memory slots associated with a given processor are unavailable if the corresponding processor socket is not populated.
- For a single DDR5 DIMM in a dual-slot channel, populate slot 1 (blue slot).
- Processor sockets are self-contained and autonomous. However, all memory subsystem support (such as memory RAS and error management) in the BIOS setup utility is applied commonly for each installed processor.
- For best system performance, memory must be installed in all eight channels for each installed processor.
- For best system performance in dual processor configurations, installed DDR5 DIMM type and population for DDR5 DIMMs configured to CPU 1 must match DDR5 DIMM type and population configured to CPU 0. For additional information, see Section 4.4.2.
- Mixing DDR5 DIMMs of different frequencies and latencies is not supported within or across processors. If a mixed configuration is encountered, the BIOS attempts to operate at the highest common frequency and the lowest latency possible.
- x4 and x8 width DIMMs may be mixed in the same channel.
- Mixing of DDR5 DIMM types (standard RDIMM, 3DS-RDIMM, 9x4 RDIMM) within or across processors is not supported. This will lead to a Fatal Error Halt during Memory Initialization.
- When populating a quad-rank DDR5 DIMM with a single- or dual-rank DDR5 DIMM in the same channel, the quad-rank DDR5 DIMM must be populated farthest from the processor. Incorrect DIMM placement results in an MRC error code. A maximum of 8 logical ranks can be used on any one channel, as well as a maximum of 10 physical ranks loaded on a channel.
- For RDIMM, 3DS-RDIMM, 9x4 RDIMM, always populate DIMMs with higher electrical loading in slot 1 (blue slot) followed by slot 2 (black slot).

4.4.1   Intel® Optane™ PMem 300 Series Module Rules

- Only Intel® Optane™ PMem 300 series modules are supported. Previous Intel® Optane™ PMem generations (such as 100 series and 200 series) are not supported.
- Intel® Optane™ PMem 300 series modules of different capacities cannot be mixed within or across processor sockets.
- Memory slots supported by Integrated Memory Controller 0 (memory channels A and B) of a given processor must be populated before memory slots on other IMCs.
- Only one Intel® Optane™ PMem 300 series module is supported per memory channel.
- Intel® Optane™ PMem 300 series modules are only supported in DIMM slot 2 (black slot) when mixed with standard RDIMM, 3DS-RDIMM, 9x4 RDIMM.
- No support for SDRAM SRx8 DIMM that is populated within the same channel as the Intel® Optane™ PMem 300 series module in any operating mode.
- Ensure that the same DDR5 DIMM type and capacity is used for each DDR5 + Intel® Optane™ PMem 300 series module combination.
- Minimum of one DDR5 DIMM per IMC (IMC 0, IMC 1, IMC 2, and IMC 3) for each installed processor.
- Minimum of one Intel® Optane™ PMem 300 series module for the board.
- Intel® Optane™ PMem 300 series modules must be populated symmetrically for each installed processor (corresponding slots populated on either side of each processor).

Table 7. Intel® Optane™ PMem 300 Series Module Support

Processor Shelf	Intel® Optane™ PMem 300 Series Capacity (GB)	Maximum Speed (MT/s)
Gold 5xxx processors	128, 256, 512	4400
Gold 6xxx Processors	128, 256, 512	4400
Platinum 8xxx processors	128, 256, 512	4400

Table 8. Standard DDR5 DIMMs Compatible with Intel® Optane™ PMem 300 Series Module

Type	Ranks per DIMM and Data Width	DIMM Size (GB) 16 Gb DRAM density
RDIMM	SRx8	16
	SRx4	32
	DRx8	32
	DRx4	64
3DS-RDIMM	QRx4 (2H)	128 (2H)
	ORx4 (2H)	256 (2H)

Note: SR = Single Rank, DR = Dual Rank, QR = Quad Rank, OR = Oct Rank, H = Stack Height.

Note: Intel® Optane™ PMem 300 series is not supported with 9x4 DDR5 DIMMs.

4.4.2   Recommended Memory Configurations

This section provides the recommended memory population configurations for the server board. For best system performance in dual-processor configurations, installed memory type and population should be the same for both processors.

See the following figure to identify the memory slot locations and the following two tables for recommended population configurations.
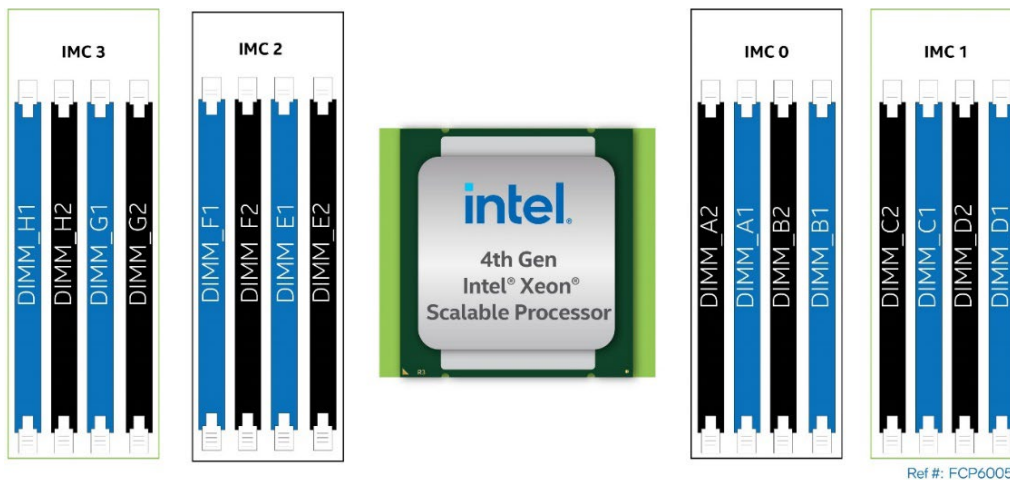
Figure 25. Memory Slot Identification

Table 9. Standard DDR5 DIMM Population Configurations per Processor

# of DIMMs	IMC 3				IMC 2				IMC 0				IMC 1			
	CH H		CH G		CH F		CH E		CH A		CH B		CH C		CH D	
	Slot 1	Slot 2	Slot1	Slot2	Slot 1	Slot 2	Slot 1	Slot 2	Slot 2	Slot 1	Slot 2	Slot 1	Slot 2	Slot 1	Slot 2	Slot 1
1	–	–	–	–	–	–	–	–	–	DDR5	–	–	–	–	–	–
	–	–	–	–	–	–	DDR5	–	–	–	–	–	–	–	–	–
	–	–	–	–	–	–	–	–	–	–	–	DDR5	–	–	–	–
	–	–	–	–	DDR5	–	–	–	–	––	–	–	–	–	–	–
2	–	–	DDR5	–	–	–	–	–	–	DDR5	–	–	–	–	–	–
	–	–	–	–	–	–	DDR5	–	–	–	–	–	–	DDR5	–	–
4	–	–	DDR5	–	–	–	DDR5	–	–	DDR5	–	–	–	DDR5	–	–
6	–	–	DDR5	–	DDR5	–	DDR5	–	–	DDR5	–	–	–	DDR5	–	DDR5
	DDR5	–	DDR5	–	–	–	DDR5	–	–	DDR5	–	DDR5	–	DDR5	–	–
	DDR5	–	–	–	DDR5	–	DDR5	–	–	–	–	DDR5	–	DDR5	–	DDR5
	DDR5	–	DDR5	–	DDR5	–	–	–	–	DDR5	–	DDR5	–	–	–	DDR5
8	DDR5	–	DDR5	–	DDR5	–	DDR5	–	–	DDR5	–	DDR5	–	DDR5	–	DDR5
12	DDR5	–	DDR5	DDR5	DDR5		DDR5	DDR5	DDR5	DDR5		DDR5	DDR5	DDR5		DDR5
	DDR5	DDR5	DDR5		DDR5	DDR5	DDR5			DDR5	DDR5	DDR5		DDR5	DDR5	DDR5
16	DDR5	DDR5	DDR5	DDR5	DDR5	DDR5	DDR5	DDR5	DDR5	DDR5	DDR5	DDR5	DDR5	DDR5	DDR5	DDR5

Table 10. DDR5 DIMM and Intel® Optane™ PMem 300 Series Population Configurations per Processor

DDR5 + PMem	Mode	IMC 3				IMC 2				IMC 0				IMC 1			
		CH H		CH G		CH F		CH E		CH A		CH B		CH C		CH D	
		Slot 1	Slot 2	Slot 1	Slot 2	Slot 1	Slot 2	Slot 1	Slot 2	Slot 2	Slot 1	Slot 2	Slot 1	Slot 2	Slot 1	Slot 2	Slot 1
4+4	1LM+AD	DDR5		PMem		DDR5		PMem			PMem		DDR5		PMem		DDR5
6+1	1LM+AD			DDR5		DDR5		DDR5			DDR5		PMem		DDR5		DDR5
8+1	1LM+AD	DDR5		DDR5		DDR5		DDR5			DDR5		DDR5		DDR5	PMem	DDR5
8+4	1LM+AD	DDR5		DDR5	PMem	DDR5		DDR5	PMem	PMem	DDR5		DDR5	PMem	DDR5		DDR5
	1LM+AD	DDR5	PMem	DDR5		DDR5	PMem	DDR5			DDR5	PMem	DDR5		DDR5	PMem	DDR5
8+8	1LM+AD	DDR5	PMem	DDR5	PMem	DDR5	PMem	DDR5	PMem	PMem	DDR5	PMem	DDR5	PMem	DDR5	PMem	DDR5
1+1[1]	1LM+AD										DDR5		PMem				

Notes: (1) Power On and Debug only. (2) AD = App Direct mode (DDR5 is 1LM (first level memory) and PMem is in App Direct mode), PMem = Persistent Memory Module.

When populating an Intel® Optane™ PMem 300 series module:

- For each individual population, rearrangements between channels are allowed if the resulting population is consistent with defined memory population rules.
- For each individual population, the same DDR5 DIMM must be used in all slots, as specified by the defined memory population rules.

4.5 Memory RAS Support

Processors within the 4th Gen Intel® Xeon® Scalable processor family support Standard or Advanced memory RAS features, defined in Table 11. Memory RAS support is dependent on the specific processor SKU installed in the server.

The following table lists the RAS features for systems configured with standard DDR5 DIMMs or a combination of standard DDR5 DIMMS and Intel® Optane™ PMem 300 series modules.

Table 11. Memory RAS Features

Memory RAS Feature	Description	Standard	Advanced
Device Data Correction	Single Device Data Correction (SDDC) via static virtual lockstep. Supported with x4 DIMMs only.	√	√
	Adaptive Data Correction: Single Region (ADC-SR) via adaptive virtual lockstep (applicable to x4 DDR5 DIMMs). Cannot be enabled with Memory Multi-Rank Sparing or Write Data CRC Check and Retry options enabled.	√	√
	Adaptive Double Data Correction: Multiple Regions (ADDDC-MR, + 1). Supported with x4 DIMMs only.	–	√
DDR5 Command/Address (CMD/ADDR) Parity Check and Retry	DDR5 technology based CMD/ADDR parity check and retry with CMD/ADDR parity error "address" logging and CMD/ADDR retry.	√	√
Memory Demand and Patrol Scrubbing	Demand scrubbing is the ability to write corrected data back to the memory once a correctable error is detected on a read transaction. Patrol scrubbing proactively searches the system memory, repairing correctable errors. Prevents accumulation of single-bit errors.	√	√
Memory Mirroring	Full memory mirroring: an intra-IMC method of keeping a duplicate (secondary or mirrored) copy of the contents of memory as a redundant backup for use if the primary memory fails. The mirrored copy of the memory is stored in memory of the same processor socket's IMC. Dynamic (without reboot) failover to the mirrored DIMMs is transparent to the operating system and applications.	√	√
	Address range/partial memory mirroring: Provides further intra-socket granularity to mirroring of memory. It provides this by allowing the firmware or operating system to determine a range of memory addresses to be mirrored, leaving the rest of the memory in the socket in non-mirror mode.	–	√
Memory Data Scrambling with Command and Address	Scrambles the data with address and command in "write cycle" and unscrambles the data in "read cycle". Addresses reliability by improving signal integrity at the physical layer. Additionally, assists with detection of an address bit error.	√	√
DDR Memory Multi–Rank Memory Sparing	Up to two ranks out of a maximum of eight ranks can be assigned as spare ranks. Cannot be enabled with ADC-SR, ADDDC-MR, +1, and Memory Mirroring options enabled.	√	√
Post Package Repair (PPR)	PPR utilizes additional spare capacity in the DDR5 that can be used to replace faulty cell areas detected during system boot time.	√	√
Partial Cache-Line Sparing (PCLS) for HBM only	Allows replacing failed single bit within a device using spare capacity available within the processor's integrated memory controller (IMC). Up to 16 failures allowed per memory channel and no more than one failure per cache line. After failure is detected, replacement is performed at a nibble level. Supported with x4 DIMMs only.	√	√

Memory RAS Feature	Description	Standard	Advanced
Memory Disable and Map Out for Fault Resilient Boot (FRB)	Allows memory initialization and booting to an operating system even when memory fault occurs.	√	√
Memory Thermal Throttling	Management controller monitors the memory DIMM temperature and can temporarily slow down the memory access rates to reduce the DIMM temperature if needed.	√	√
MEMHOT Pin Support for Error Reporting	The MEMHOT pin can be configured as an output and used to notify if DIMM is operating outside of the target temperature range. Used to implement the memory thermal throttling feature.	√	√

Make sure to follow these rules for memory RAS population and BIOS setup utility:

- Memory sparing and memory mirroring options are enabled in the BIOS setup utility.
- Memory sparing and memory mirroring options are mutually exclusive in this product. Only one operating mode at a time may be selected in the BIOS setup utility.
- If a RAS mode has been enabled and the memory configuration is not able to support it during boot, the system falls back to independent channel mode and log and display errors.
- Rank sparing mode is only possible when all channels that are populated with memory have at least two single-rank or double-rank DIMMs installed, or at least one quad-rank DIMM installed on each populated channel.
- Memory mirroring mode requires that for any channel pair that is populated with memory, the memory population on both channels of the pair must be identically sized.
- The Intel® Optane™ PMem 300 series RAS features listed in the following table are integrated into the system memory RAS features.

The following table lists additional memory RAS features specific to the Intel® Optane™ PMem 300 series memory. These features are managed by the processor's IMC.

Table 12. Intel® Optane™ PMem 300 Series RAS Features

Memory RAS Feature	Description
DIMM Error Detection and Correction	Protects against random bit failures across media devices.
DIMM Patrol Scrubbing	Proactively searches the DIMM memory, repairing correctable errors. This capability can prevent correctable errors from becoming uncorrectable due to accumulation of failed bits.
DIMM Address Error Detection	Ensures the correctness of addresses when data is read from media devices.
DIMM Data Poisoning	Mechanism to contain, and possibly recover from, uncorrectable data errors. Depending on the mode used, poisoning has different reset behavior: • In App Direct, poison is not cleared with reset.
DIMM Viral	Ensures that potentially corrupted data is not committed to persistent memory in App Direct and is supported only in tandem with poison. Viral mode only applies to App Direct mode.
Poison List Management	Hardware / Firmware enhancement to Address Range Scrub (ARS) designed to reduce the latency of ARS execution on the PMem module.
DIMM Address Range Scrub (ARS)	Obtains the healthy memory media range before assigning it to a persistent memory region.
DDR-T2 Command and Address Parity Check and Retry	Host retries a CMD/ADDR transaction if the DIMM controller detects a parity error and initiates an error flow.
DDR-T2 Read Write Data ECC Check and Retry	Host continuously retries a data transaction if the DIMM controller detects an ECC error and initiates an error flow.
Faulty DIMM Isolation	Identifies a specific failing DIMM enabling replacement of only the DIMM that has failed.

The Intel® Server Board M50FCP2BSTD supports Intel® Software Guard Extensions (Intel® SGX) and Intel® Total Memory Encryption – Multi-Key (Intel® TME-MK) technologies. When any of these technologies are enabled, Intel® Optane™ PMem 300 series is disabled. Intel® SGX for system servers works with all basic memory RAS features. In Intel® SGX mode, the following advanced RAS features are not supported by the 4th Gen Intel® Xeon® Scalable processors family. Refer to 4th Gen Intel® Xeon® Scalable processors family *BIOS Firmware External Product Specification (EPS) for more information.*

- Machine check architecture (MCA) recovery.
- Enhanced MCA generation 2 (EMCA2).
- Intel® Ultra Path Interconnect (Intel® UPI) dynamic link width reduction.
- DMI2/PCH failover.
- CPU online/offline.
- Intel® UPI online/offline.
- Dynamic partitioning.
- Memory bank sparing.
- Adaptive double device data correction (ADDDC).
- Memory mirroring.
- Address-based memory mirroring.

5. System Firmware and Utilities

The server board includes a system software stack that consists of the components included in the following list. Together, they configure and manage features and functions of the server system.

- System BIOS
- BMC firmware
- Intel® Management Engine (Intel® ME) firmware / Intel® Server Platform Services (Intel® SPS)
- Field replacement unit (FRU)
- Intel® Platform Controller Hub Ignition Firmware (Intel® PCH Ignition Firmware)

These features and functions of the server system are managed jointly by the BIOS and the BMC firmware:

- Intelligent Platform Management Interface (IPMI) watchdog timer
- Messaging support, including command bridging and user/session support
- BIOS boot flags support
- Event receiver device: The BMC receives and processes events from the BIOS
- Serial-over-LAN (SOL)
- ACPI state synchronization: The BMC tracks ACPI state changes that are provided by the BIOS
- Fault resilient boot (FRB): FBR level 2 (FRB-2) is supported by the watchdog timer functionality
- Integrated KVM (Keyboard, Video, and Mouse)
- Integrated remote media redirection
- DIMM temperature monitoring: new sensors and improved acoustic management using closed-loop fan control algorithm facilitates accurate DIMM temperature reading
- Intel® Intelligent Power Node Manager support
- Sensor and SEL logging additions/enhancements (such as, additional thermal monitoring capability)
- Embedded platform debug feature that allows capture of detailed data for later analysis by Intel
- Intel® PCH Ignition Firmware supports platform boot and security features. Delivered as configurable binary with small footprint

Note: Front panel management: In an Intel® Server System M50FCP2UR and M50FCP1UR, the BMC controls the system status LED and chassis ID LED. It supports secure lockout of certain front panel functionality and monitors button presses. The chassis ID LED is turned on using a front panel button or a command.

A factory installed firmware stack is pre-programmed on the server board during the board assembly process, making the server board functional at first power on. However, to ensure the most reliable system operation, Intel highly recommends checking http://downloadcenter.intel.com for the latest available system updates and apply them before production deployment.

System updates can be performed in several operating environments, either in the UEFI shell using the UEFI-only System Update Package (SUP), or under different operating systems using the Single-boot Firmware Update Package (SFUP) utility.

See the following Intel® documents for more in -depth information about the system software stack and its functions:

- BIOS Firmware External Product Specification (EPS) – Intel® NDA required
- Integrated Baseboard Management Controller Firmware External Product Specification (EPS) – Intel® NDA Required

5.1   Hot Keys Supported during POST

Certain hot keys are recognized during power-on self-test (POST). A hot key is a keyboard key or key combination that is recognized as an unprompted command input. In most cases, hot keys are recognized even while other processing is in progress.

BIOS supported hot keys are only recognized by the system BIOS during the system boot time POST process. Once the POST process has completed and transitions the system boot process to the operating system, BIOS supported hot keys are no longer recognized.

The following table provides a list of available POST hot keys along with a description for each.

Table 13. POST Hot Keys

Hot Key	Function
<F2>	Enter the BIOS setup utility
<F6>	Pop-up BIOS boot menu
<F12>	Network boot
<Esc>	Switch from logo screen to diagnostic screen
<Pause>	Stop POST temporarily (press any key to resume)

5.1.1   POST Logo/Diagnostic Screen

If Quiet Boot is enabled in the BIOS setup utility, a splash screen is displayed with the standard Intel logo screen or a customized original equipment manufacturer (OEM) logo screen, if one is present, in the designated flash memory location. By default, Quiet Boot is enabled in the BIOS setup utility and the logo screen is the default POST display. However, pressing **<Esc>** hides the logo screen and displays the diagnostic screen instead during the current boot.

If a logo is not present in the BIOS flash memory space, or if Quiet Boot is disabled in the system configuration, the POST diagnostic screen is displayed with a summary of system configuration information. The POST diagnostic screen is purely a text mode screen, as opposed to the graphics mode logo screen.

If console redirection is enabled in the BIOS setup utility, the Quiet Boot setting is disregarded, and the text mode diagnostic screen is displayed unconditionally. This action is due to the limitations of console redirection that transfers data in a mode that is not graphics compatible.

5.1.2   BIOS Boot Pop-Up Menu

The BIOS boot selection (BBS) menu provides a boot device pop-up menu that is invoked by pressing the **<F6>** key during POST. The BBS pop-up menu displays all available boot devices. The boot order in the dialog box box is different from the boot order in the BIOS setup utility. The pop-up menu lists all the available devices from which the system can be booted and allows a manual selection of the desired boot device.

When an administrator password is configured in the BIOS Setup utility, the administrator password is required to access the boot pop-up menu. If a user password is entered, the user is taken directly to the boot manager in the BIOS setup utility, only allowing booting in the order previously defined by the administrator.

5.1.3   Entering the BIOS Setup Utility

To enter the BIOS setup utility using a keyboard (or emulated keyboard), press the **<F2>** function key during boot time when the OEM or Intel logo screen or the POST diagnostic screen is displayed.

The following instructional message is displayed on the diagnostic screen or above the Quiet Boot logo screen:

> Press [Enter] to directly boot.
> Press [F2] to enter setup and select boot options.
> Press [F6] to show boot menu options.
> Press [F12] to boot from network.

Note: With a USB keyboard, it is important to wait until the BIOS indicates the keyboard discovery by emitting short beeps. Until the USB controller has been initialized and the keyboard activated, key presses are not read by the system.

The top-level menu of the BIOS Setup utility is displayed initially. However, if a serious error occurs during POST, the system enters the Error Manager screen instead of the top-level menu screen. For additional BIOS setup utility information, see the *BIOS Setup Utility User Guide*.

5.1.4 BIOS Update Capability

To bring BIOS fixes or new features into the system, it is necessary to replace the currently installed BIOS image with an updated one. Full BIOS update instructions are provided with update packages downloaded from the Intel® website.

5.2 System Update Package (SUP) for Intel® Server System M50FCP2SBSTD

The SUP is a set of UEFI-based utilities and files bundled together and used to update the system BIOS and other embedded system firmware. Included within the compressed file package is a *README* file providing complete system update instructions and a STARTUP.NSH script file that automates the entire system update process with little or no user intervention. The latest SUP can be downloaded from: http://downloadcenter.intel.com.

5.3 Intel® Server Configuration Utility

The Intel® Server Configuration Utility is a command-line tool that supports the following features:

- Save selected BIOS and/or firmware settings to a file
- Write BIOS and firmware settings from a file to a server
- Configure selected firmware settings
- Configure selected BIOS settings
- Configure selected system settings
- Display selected firmware settings
- Display selected BIOS settings

For further Intel® Server Configuration Utility information, see the *Intel® Server Configuration Utility User Guide*.

5.4 Intel® Server Firmware Update Utility

The Intel® Server Firmware Update Utility is used for updating the system firmware. The utility is available in different versions for different operating systems such as UEFI, Windows*, and Linux*. The Utility supports the following features:

- Updates the Basic Input/Output System (BIOS) firmware using the Intel® Platform Firmware Resilience (Intel® PFR) technology. The utility transfers the content of the firmware binary file to a temporary storage and the real update starts on the next boot.
- Updates the Intel® Server Management firmware of the baseboard management controller (BMC). The new firmware is loaded to the BMC on the next BMC boot.

- Updates Complex Programmable Logic Device (CPLD).
- Supports customized firmware update using the Intel® Integrator Toolkit.
- Updates Non-volatile RAM (NVRAM).
- Executes Recovery update.
- Updates the field replaceable units (FRUs) in the system's NVRAM and sensor data
- Records (SDR) in the BMC staging area.
- Allows specific FRU field modifications.
- Displays information about: BIOS, BMC, baseboard, FRU, SDR, system management BIOS
- (SMBIOS), and/or Intel® Management Engine (Intel® ME).
- Restores the BIOS default settings.
- Clears BIOS customized settings.
- Changes the splash screen logo picture in BIOS.

For further Intel® Server Firmware Update Utility information, see the *Intel® Server Firmware Update Utility User Guide.*

5.5 Intel® Server Information Retrieval Utility

The Intel® Server Configuration Utility is a command-line tool that can be used to display and/or set a variety of system BIOS and firmware settings. In addition, the utility can be used to save system settings or restore them from a file. The Intel® Server Configuration Utility is available for different operating systems, like UEFI, Windows*, and Linux*. The utility collects the following system information and writes the data to a log file.

- Platform firmware inventory
- Sensors
- Sensor data records (SDR)
- Baseboard FRU
- System boot order
- BMC user settings
- BMC LAN channel settings
- BMC SOL channel settings
- BMC power restore policy settings
- BMC channel settings
- SMBIOS (type 1, type 2, type 3)
- Memory
- Processor
- Storage devices –hard disk drives (HDDs) and solid-state drives (SSDs)
- Operating system information
- Device manager information (such as drivers)
- List of software installed
- Operating system event log
- PCI bus device information
- RAID settings and RAID log
- BIOS settings (per the BIOS setup utility)

For further Intel® Server Information Retrieval Utility information, refer to the *Intel® Server Information Retrieval Utility User Guide.*

5.6 Intel® Server Debug and Provisioning Tool (Intel® SDP Tool)

The Intel® Server Debug and Provisioning Tool (Intel® SDP Tool) is a single server command line tool that communicates with the BMC out-of-band to perform debug and provisioning tasks. It does not require any agents, operating system or host network on the remote server and can be scripted to run on multiple systems at the same time. The tool is also used by Intel® Data Center Manager and other software plugins to perform provisioning tasks. For additional information about the Intel® Server Debug and Provisioning Tool, refer to the Intel® Server Debug and Provisioning Tool User Guide.

Supported features include:

- Update BMC, BIOS, Intel® ME, and SDR
- Deploy an EFI based custom payload. Custom payloads can perform firmware updates of other components, configure RAID or collect logs
- Configure BIOS and BMC settings
- Download/view system event log, sensors, and debug logs
- Mount virtual media images (ISO and USB)
- Check online for latest BIOS and BMC versions for given platform
- View system inventory (CPU, memory, storage, networking)
- View firmware versions and perform power actions

6. Server Management

The Intel® Server Board M50FCP2SBSTD uses the baseboard management controller (BMC) features of an Aspeed AST2600* server management processor (SMP). The BMC supports multiple system management features including intra-system sensor monitoring, fan speed control, system power management, and system error handling and messaging. It also provides remote platform management capabilities including remote access, monitoring, logging, and alerting features.

All server management capabilities can be split in two groups:

- Standard management features (Included)
- Optional advanced management features that can be enabled with the purchase of advanced management license key

In addition, BMC integrates with the Intel® Data Center Manager (DCM) software to provide unified management at Data Center level.

6.1 Remote Management Port

The Intel® Server Board M50FCP2SBSTD includes a Remote Management Port used to remotely access embedded system management features. The Remote Management Port is an RJ45 Gigabit Ethernet port on the back edge of the server board.

Note: This Ethernet port is dedicated for system management purposes only. It is not intended or designed to support standard LAN data traffic.
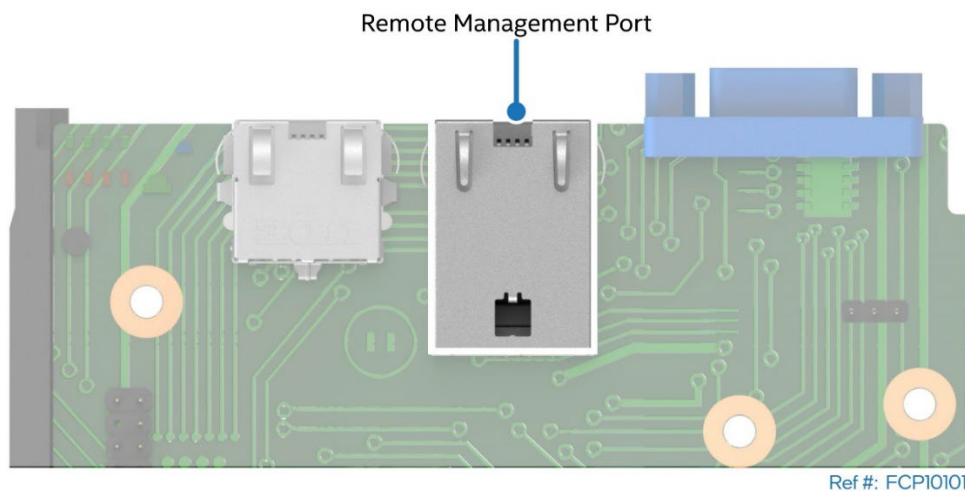
Figure 26. Remote Management Port

The remote management port can be configured using the <F2> BIOS Setup Utility before it can be used for remote management purposes.

6.1.1   Configuring Server Management Port Using the BIOS Setup Utility

1. During the power-on self-test (POST), press **<F2>** to access the Main page of the embedded BIOS setup utility.
2. Navigate to the **Server Management** tab and select **BMC LAN Configuration** to enter the BMC LAN Configuration screen (see Figure 27).
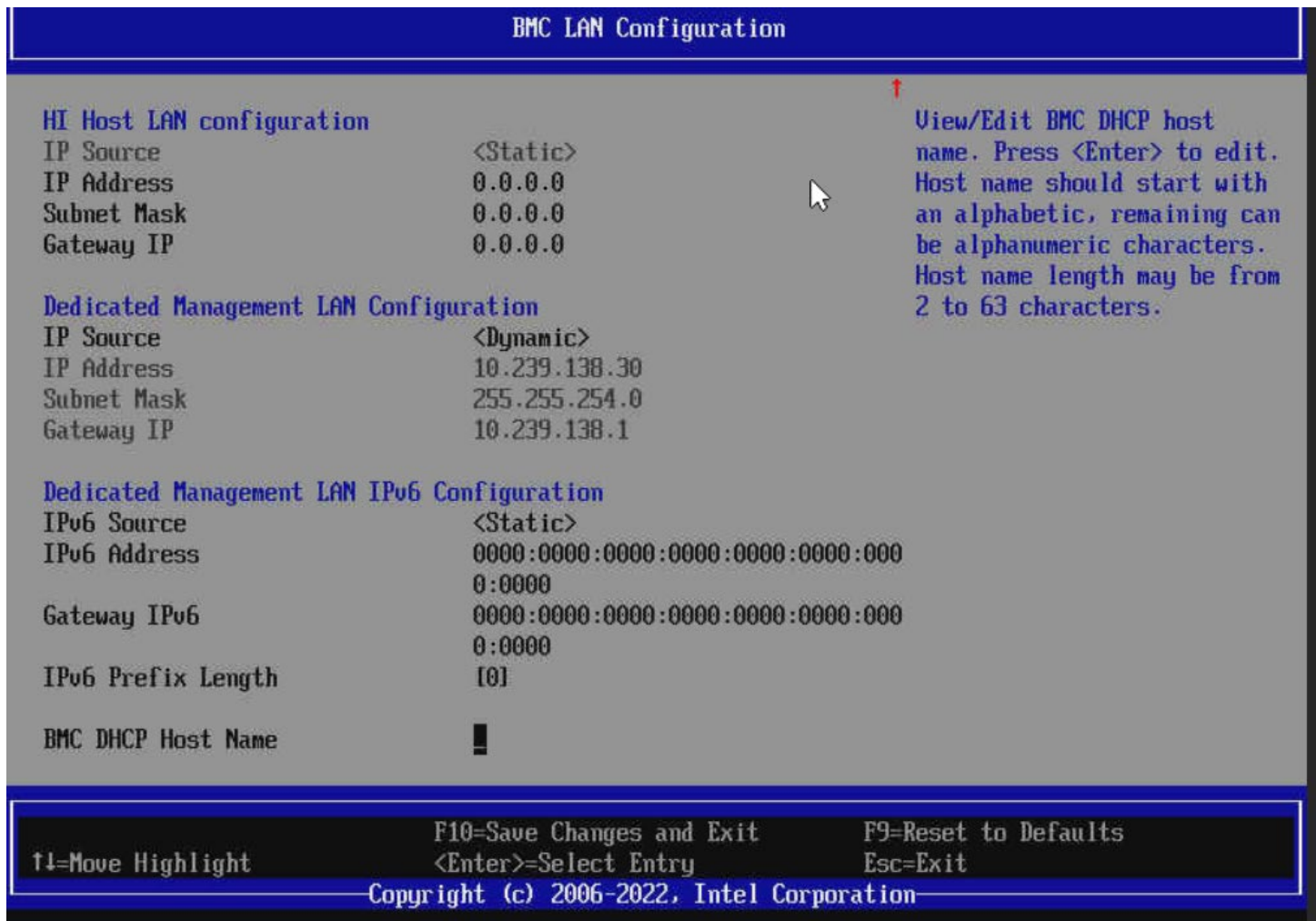
Figure 27. BMC LAN Configuration Screen of the BIOS Setup Utility

3. For an IPv4 network:
   - If configuring the server management BMC LAN, scroll down to **Dedicated Management LAN Configuration**> **IP source** and then select either **Static** or **Dynamic**. If **Static** is selected, configure the **IP address**, **Subnet mask**, and **Gateway IP** as needed.
4. For an IPv6 network:
   - If configuring the server management BMC LAN, scroll to **Baseboard LAN IPv6 configuration** > **IP source** and then select **Enabled**. Then scroll to **IPV6 source** and select either **Static** or **Dynamic**. If **Static** is selected, configure the **IPV6 address**, **Gateway IPV6**, and **IPV6 Prefix Length** as needed.
5. Navigate back to the **Server Management** tab then select **User Configuration** to enter the User Configuration screen (Figure 28).
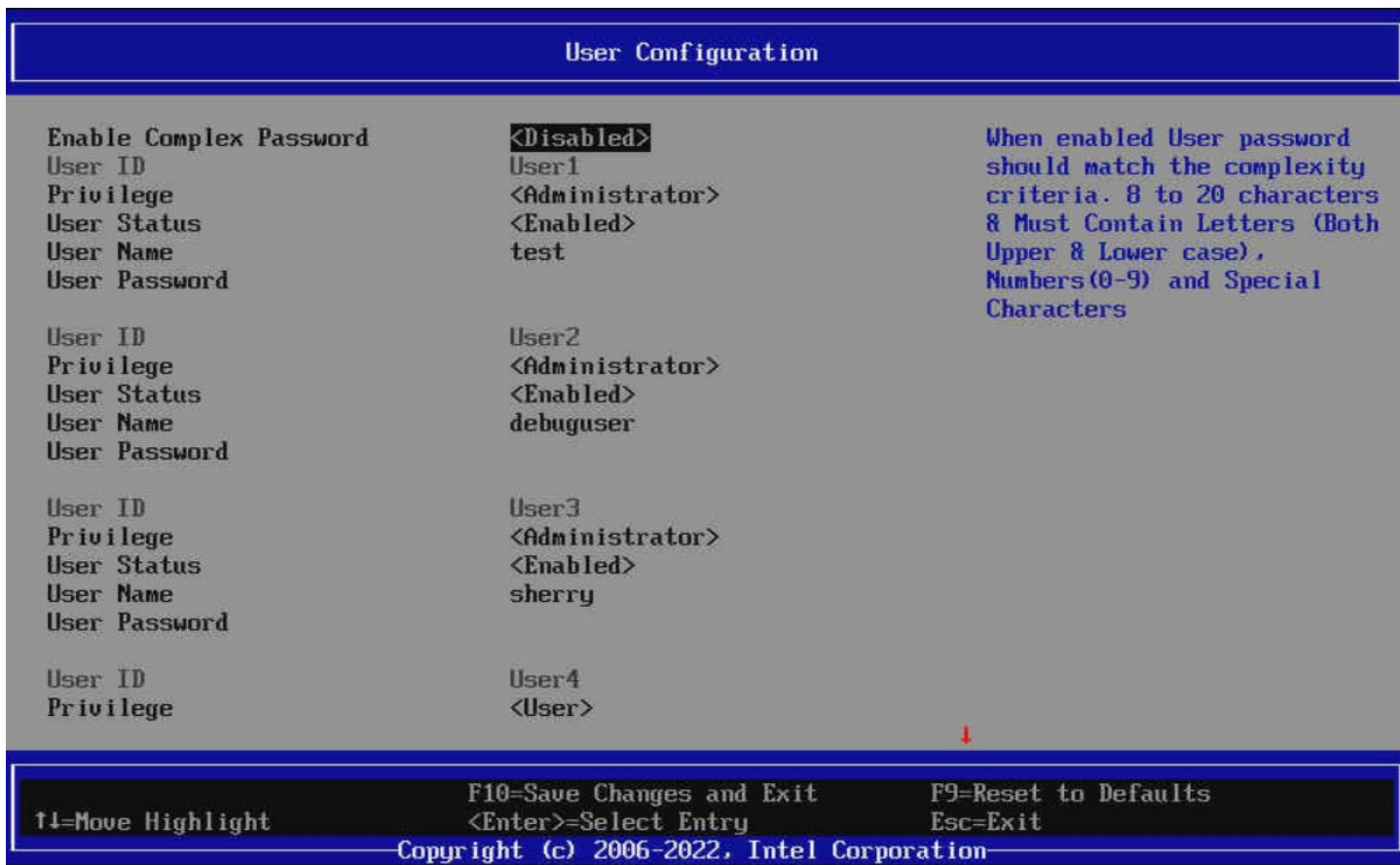
Figure 28. User Configuration Screen of the BIOS Setup Utility

6. Under a **User ID**, enter a **User Name**

7. Press **<F10>** to save the configured settings and exit the BIOS setup utility

8. Reboot the server and re-enter the <F2> BIOS Setup Utility (See the Notes section on the following page)

9. Navigate back to the **Server Management** tab and select **User Configuration**

10. Under the selected **User ID** configure the following settings: (See the Notes section on the following page)

    o Privilege – Select the privilege to be used. Administrator privilege is required to use KVM or media redirection enabled by the advanced management features.

    o User status – Select Enabled.

    o User password – Enter the desired password twice.

11. Press **<F10>** to save the configured settings and exit the BIOS setup utility. Reboot the server to use LAN ports with configured settings.

Notes:
- The User Name must be entered and saved before any additional User ID options can be configured. To save the User Name data, the BIOS Utility must be exited, and the system must be rebooted, to re-enter the BIOS Utility.
- User names cannot be saved as "Null", or "root", or match any other existing user names.
- User names cannot exceed 16 characters and passwords cannot exceed 20 characters

Once the management port is configured, the server can be accessed remotely to perform system management features defined in the following sections.

6.2 Standard Server Management Features

The following server management features are supported on the Intel® Server Board M50FCP2SBSTD by default.

- Integrated BMC Web Console
- Virtual KVM over HTML5
- Redfish*
- Support for IPMI 2.0 and Intel® Node Manager (Intel® NM)
- Out-of-band BIOS/BMC update and configuration
- System inventory
- Autonomous debug log

The following subsections provide a brief description for each feature.

6.2.1 Integrated BMC Web Console

The BMC firmware includes an embedded web server that can serve web pages to any supported browser. This web console is designed to be a fully functional server administration tool allowing a system administrator to:

- View system information including firmware versions, server health, diagnostic information, and power statistics.
- Configure BMC and BIOS options
- Perform power actions (power on, power off, etc.)
- Launch the KVM and media redirection application

Enter the IP address of the BMC management port into the web browser to open the Integrated BMC Web Console login page (See Figure 29).

Enter the username and password and select a language option. For example:

- Username: `<choose any username other than root>`
- Password: `<choose a password unique to the system>`
- Language: **English**

For additional information about the BMC Web Console, refer to the Intel® Integrated Baseboard Management Controller Web Console (Intel® BMC Web Console) User Guide.
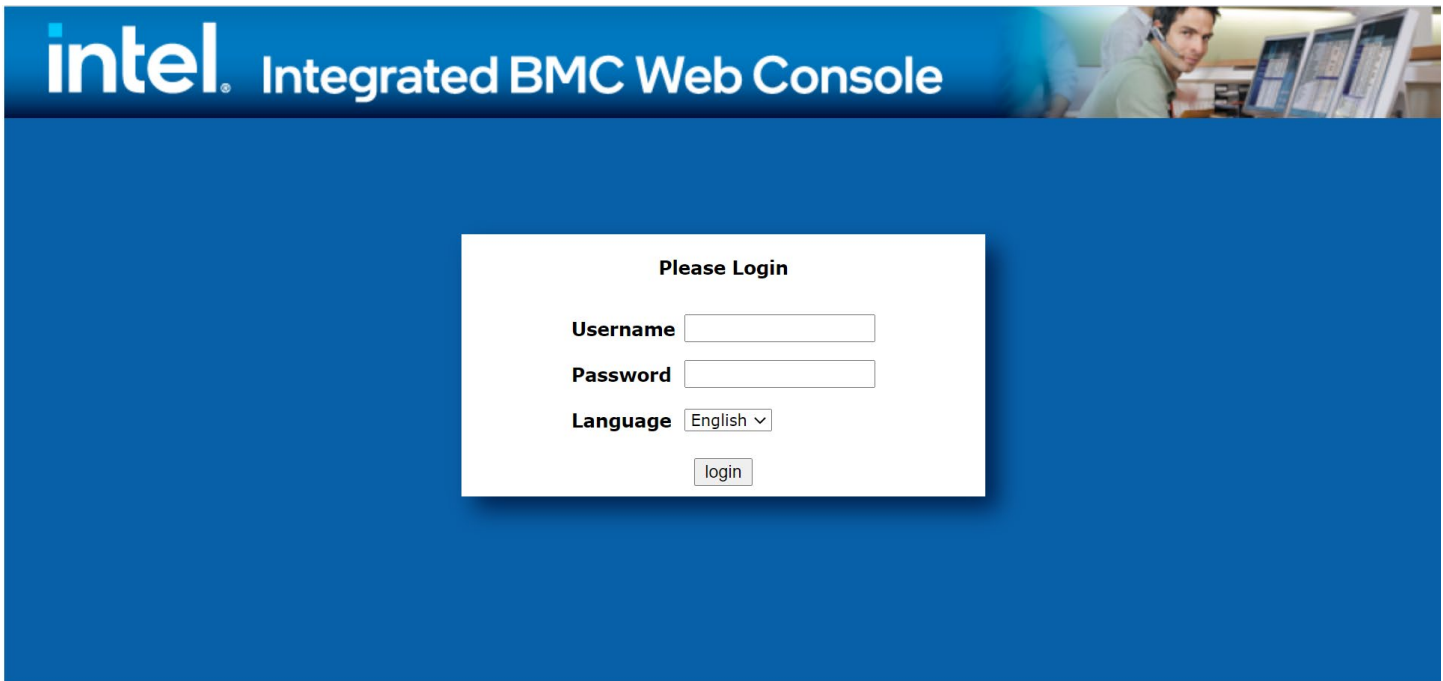
Figure 29. Integrated BMC Web Console Login Page

Click the **Login** button to view the home page.
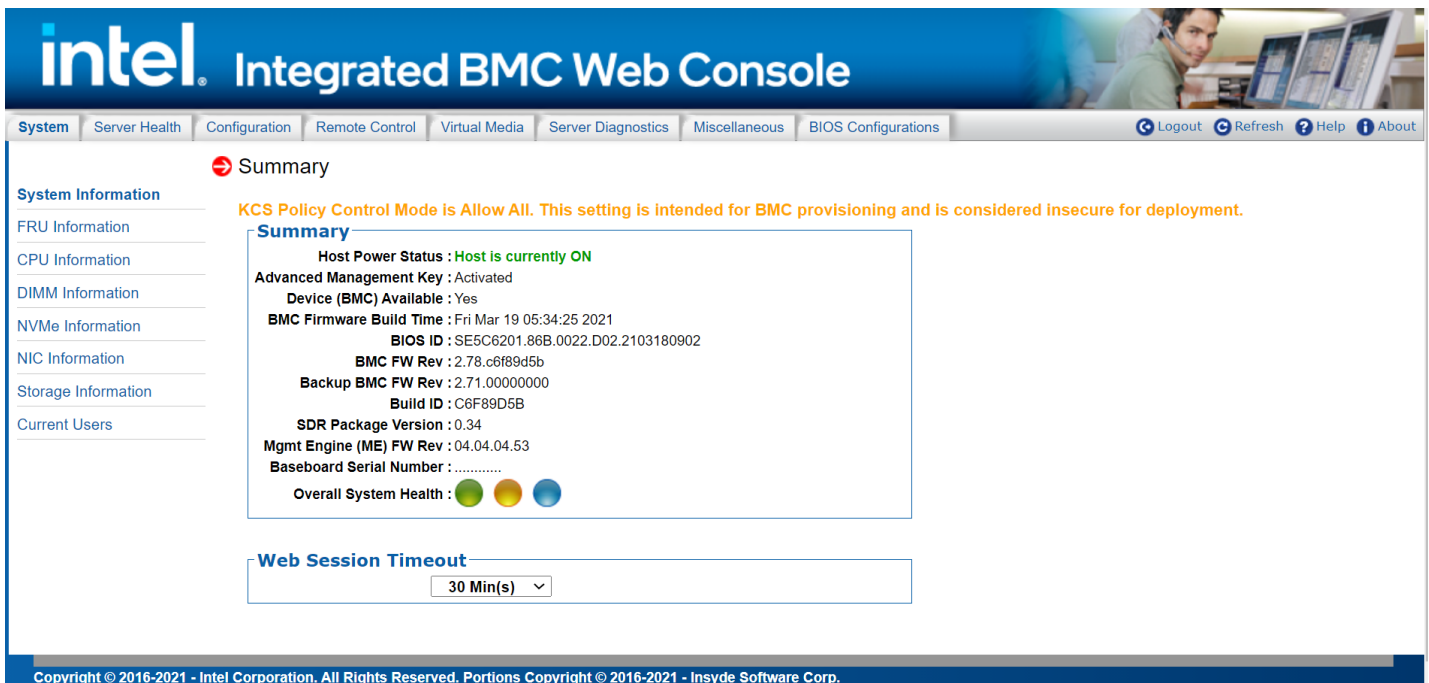
Figure 30. Integrated BMC Web Console: System Tab View

6.2.2   Virtual KVM over HTML5

The BMC firmware supports keyboard, video, and mouse redirection (KVM) over LAN. This feature is available as an HTML5 application of the embedded web server and allows a user to interact with a remote server using the keyboard, video, and mouse (KVM) of the local computer as if the user were physically present at the managed server. USB1.1 or USB 2.0 based mouse and keyboard redirection are supported. It is also possible to use the KVM-redirection (KVM-r) session concurrently with media-redirection (media-r).

The KVM redirection application supports the following keyboard layouts: English, Chinese (traditional), Japanese, German, French, Spanish, Korean, Italian, and United Kingdom. The application also includes a "soft keyboard" function. This is used to simulate an entire keyboard on the screen. The "soft keyboard" functionality supports the following layouts: English, Dutch, French, German, Italian, Russian, and Spanish.

The KVM-redirection feature automatically senses video resolution for best possible screen capture and provides high-performance mouse tracking and synchronization. It allows remote viewing and configuration in pre-boot POST and BIOS setup utility once BIOS has initialized video.

6.2.3   Redfish* Support

Distributed Management Task Force's (DMTF) Redfish® is a standard designed to deliver simple and secure management for converged, hybrid IT and the Software Defined Data Center (SDDC). Both human readable and machine capable, Redfish leverages common Internet and web services standards to expose information directly to the modern tool chain. The BMC currently supports version 1.7 and schema version 2019.1.

6.2.4   Intelligent Platform Management Interface (IPMI) 2.0 Support

The BMC is IPMI 2.0 compliant including support for Intel® Dynamic Power Node Manager. IPMI defines a set of interfaces used by system administrators for out-of-band management of computer systems and monitoring of their operation.

6.2.5   Out-of-band BIOS / BMC Update and Configuration

The BMC allows administrators to update the BMC, BIOS, and CPLD firmware using either Redfish* schemas or embedded web console. The BMC firmware also includes Power Supply and hot swap back plane (HSBP) firmware modules. The firmware images are loaded into BMC staging area and programmed into a SPI flash under control of PFR on next reboot.

The BMC also supports Redfish schemas to view and modify BIOS settings. On each boot, the BIOS provides all its settings and active value to the BMC to be displayed. BIOS also checks if any changes are requested and performs those changes.

6.2.6   System Inventory

The BMC supports Redfish schemas and embedded web console pages to display system inventory. This inventory includes FRU information, processor, memory, NVMe, networking, and storage. When applicable, the firmware version is also provided.

6.2.7   Autonomous Debug Log

The BMC collects and stores information from different server subsystems:
- Configuration data about SDR, BMC, PCIe, power supply including power supply "black box" data
- SMBIOS data
- System Event Log (SEL)
- POST codes from the last two system boots

When the system has a catastrophic error condition leading to a system shutdown, the BMC will also collect processor machine check registers, memory controller machine check registers, I/O global error registers, and other processor state info. All this information can be retrieved as a single archive called Debug Log from the Integrated Web Console or using syscfg and SDPTool utilities.

6.2.8   Security Features

The BMC supports several security features including OpenLDAP and Active Directory, security logs, ability to turn off any remote port, Secure Sockets Layer (SSL) certificate upload, VLAN support, and KCS control. The BMC also supports full user management with password defined privileges and with the ability to define password complexity rules. Each BMC release is given a security version number to prevent firmware downgrades from going to lower security versions.

Intel® provides a best practices security guide, available at:
https://www.intel.com/content/www/us/en/support/articles/000055785/server-products.html

6.3   Advanced Server Management Features

Purchasing an optional Advanced System Management product key (iPC **ADVSYSMGMTKEY**) unlocks the following advanced system management features:

- Virtual Media Local Image Redirection (HTML5 and Java)
- Virtual Media shared files and folders redirection
- Out-of-band hardware RAID Management for latest Intel® RAID cards
- Included single system license for Intel® Data Center Manager (Intel® DCM)
    - o   Intel® Data Center Manager (Intel® DCM) is a software solution that collects and analyzes the real-time health, power, and thermals of a variety of devices in data centers helping you improve the efficiency and uptime. For more information, go to https://www.intel.com/content/www/us/en/software/intel-dcm-product-detail.html

The Advanced System Management product key can be purchased and pre-loaded onto the system when ordering a fully integrated server system directly from Intel® using its online Configure-to-Order (CTO) tool. The Advanced System Management product key can also be purchased separately and installed later.

When purchasing the product key separately from the system, instructions are provided on where to register the product key with Intel. A license file is then downloaded onto the system where the Integrated BMC Web Console or the Intel® Server Configuration utility is used to upload the key to the BMC firmware to unlock the advanced features.

6.3.1   Virtual Media Local Image Redirection (HTML5)

The BMC supports media redirection of local IMG, IMA or ISO image files. This redirection is supported in HTML5 remote console clients. When a user selects the "Launch Window to Mount Local Image" option, a new web page is displayed. The page provides the user interface to select the type of source media (image files) and the location of the desired media to make it available to the remote server system.

After the type and specific media are selected, the interface provides a mount/unmount interface so the user can connect the media to or disconnect the media from the server system. Once connected, the selected image file is presented to the server system as a read-only removable media and may be interacted like a CD-ROM drive.

This feature gives system administrators the ability to install software (including operating system), copy files, perform firmware updates, from the local media on their workstation.

Note: The shared file is presented to the server system as a UDF file system. The operating system of the server must be able to interact with UDF file systems for this feature to work.

6.3.2   Virtual Media Shared Files and Folders Redirection

In addition to supporting virtual media redirection from the administrator's workstation (see Section 6.3.1), the BMC also supports media redirection of .IMG, .IMA or .ISO files hosted on a file server, accessible to the BMC over network interface.

The current version supports Samba shares (Microsoft Windows file shares) and NFS shares. This virtual media redirection is more effective for mounting virtual media at scale, instead of processing all files from the workstation's drive through the HTML5 application and over the workstation's network. Each BMC makes a direct network file share connection to the file server and accesses files across that network share directly.

6.4 Intel® Data Center Manager (Intel® DCM) Support

Intel® DCM is a solution for out-of-band monitoring and managing the health, power, and thermals of servers and a variety of other types of devices.

What can you do with Intel® DCM?

- Automate health monitoring
- Improve system manageability
- Simplify capacity planning
- Identify underutilized servers
- Measure energy use by device
- Pinpoint power/thermal issues
- Create power-aware job scheduling tasks
- Increase rack densities
- Set power policies and caps
- Improve data center thermal profile
- Optimize application power consumption
- Avoid expensive PDUs and smart power strips

For more information, go to

https://www.intel.com/content/www/us/en/software/intel-dcm-product-detail.html

Note: See Section 1.1 for references to the *Intel® Data Center Manager (Intel® DCM) Product Brief* and *Intel® Data Center Manager (Intel® DCM) Console User Guide.*

7.   Server Board Connector / Header Pinout Definition

This chapter identifies the location and pinout for most server board connectors and headers on the server board. Information for some connectors and headers is found elsewhere in the document where the feature is described in more detail.

Pinout definitions for the following server board connectors are only made available by obtaining the board schematics directly from Intel (NDA required).

- All riser slots
- OCP module connector
- M.2 SSD connectors
- Memory module slots
- Processor sockets

Note: See Appendix F for a list of connectors / headers used on the server board. The appendix provides a list of manufacturers and part numbers.

7.1   Power Connectors

The server board includes several power connectors that are used to provide DC power to various devices.

7.1.1   Main Power Connectors

Main server board power is supplied from two slot 50-pin connectors that allow support for one or two CRPS type power supplies to dock directly to the server board. The connectors are labeled "MAIN PWR 1" and "MAIN PWR 2" on the server board as shown in the following figure.

The server board provides no option to support power supplies with cable harnesses. In a 1+1 redundant power supply configuration, a failed power supply module is hot-swappable. Table 14 provides the pinout for the "MAIN PWR 1" and "MAIN PWR 2" connectors.
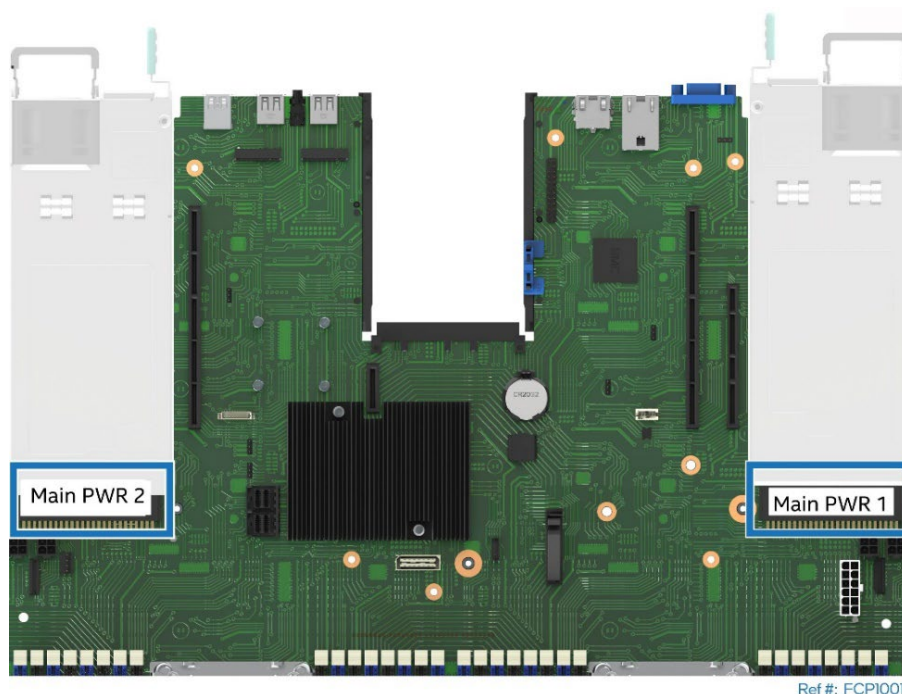
Figure 31. "MAIN PWR 1" and "MAIN PWR 2" Connectors

Table 14. Main Power (Slot 1) and Main Power (Slot 2) Connector Pinout ("MAIN PWR 1" and "MAIN PWR 2")

Pin #	Signal Name	Pin #	Signal Name
B1	GROUND	A1	GROUND
B2	GROUND	A2	GROUND
B3	GROUND	A3	GROUND
B4	GROUND	A4	GROUND
B5	GROUND	A5	GROUND
B6	GROUND	A6	GROUND
B7	GROUND	A7	GROUND
B8	GROUND	A8	GROUND
B9	GROUND	A9	GROUND
B10	P12V	A10	P12V
B11	P12V	A11	P12V
B12	P12V	A12	P12V
B13	P12V	A13	P12V
B14	P12V	A14	P12V
B15	P12V	A15	P12V
B16	P12V	A16	P12V
B17	P12V	A17	P12V
B18	P12V	A18	P12V
B19	P3V3_AUX: PD_PS1_FRU_A0	A19	SMB_PMBUS_DATA_R
B20	P3V3_AUX: PD_PS1_FRU_A1	A20	SMB_PMBUS_CLK_R
B21	P12V_STBY	A21	FM_PS_EN_PSU_N
B22	FM_PS_CR1	A22	IRQ_SML1_PMBUS_ALERTR2_N
B23	P12V_SHARE	A23	ISENSE_P12V_SENSE_RTN
B24	TP_1_B24 (for MAIN PWR 1) TP_2_B24 (for "MAIN PWR 2)	A24	ISENSE_P12V_SENSE
B25	FM_PS_COMPATIBILITY_BUS	A25	PWRGD_PS_PWROK

7.1.2   Hot Swap Backplane Power Connector

The server board includes one white 2x6-pin power connector that, when cabled, provides power for hot swap backplanes, as shown in Figure 32. On the server board, this connector is labeled "HSBP PWR".

HSBP Power Connector (HSBP PWR)

Ref #: FCP10110
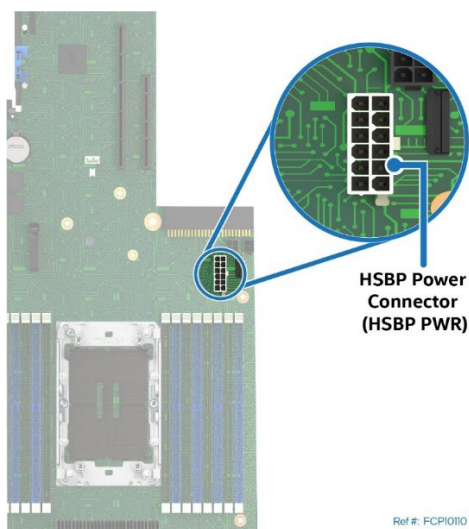
Figure 32. Hot Swap Backplane Power Connector

Table 15. Hot Swap Backplane Power Connector Pinout ("HSBP PWR")

Pin #	Signal Name	Pin #	Signal Name
1	GND	7	P12V_240VA3
2	GND	8	P12V_240VA3
3	GND	9	P12V_240VA2
4	GND	10	P12V_240VA2
5	GND	11	P12V_240VA1
6	GND	12	P12V_240VA1

7.1.3   Optional 12-V Power Connectors

The server board includes five 2x2-pin power connectors labeled "OPT_12V_PWR" (See Figure 33). The connectors provide supplemental 12 V power-out to high-power PCIe x16 add-in cards with power requirements that exceed the 75 W maximum power supplied by the riser card slot.

A cable from the connectors may be routed to a power-in connector on the given add-in card. Maximum power draw for each connector is 225 W. Maximum power is also limited by available power provided by the power supply and the total power draw of the given system configuration.

A power budget calculation for the complete system should be performed to determine how much supplemental power is available to support any high-power add-in cards.
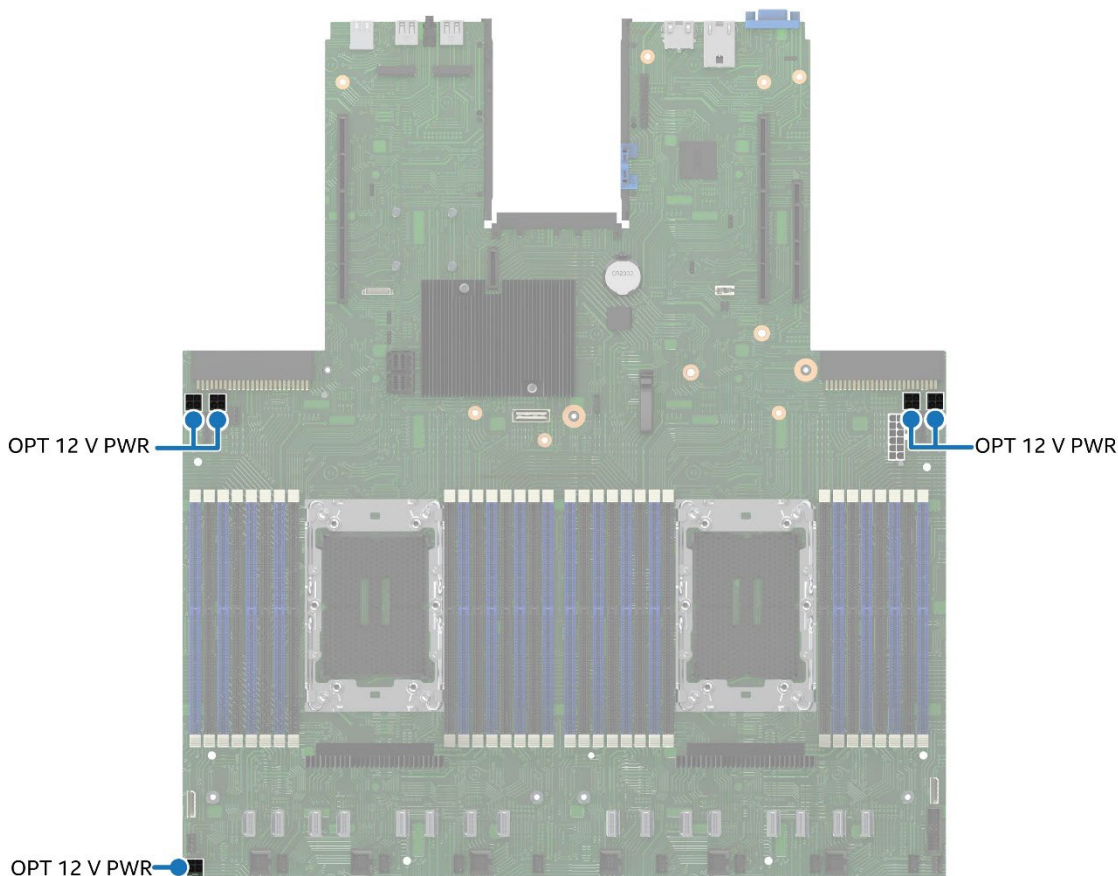
Ref #: FCP10031

Figure 33. Auxiliary Power Connectors

The following table provides the pinout of the 12-V power connectors.

Table 16. Riser Slot Auxiliary Power Connector Pinout

Pin #	Signal Name
1	GROUND
2	GROUND
3	P12V
4	P12V

7.1.4   Peripheral Power Connector

The server board includes one 4-pin power connector intended to provide power for peripheral devices such as solid-state devices (SSDs). The power connector supports 5 and 12 volts. On the server board, this connector is labeled "Peripheral_ PWR".

5/12 V PWR Connector

Ref #: FCP10150
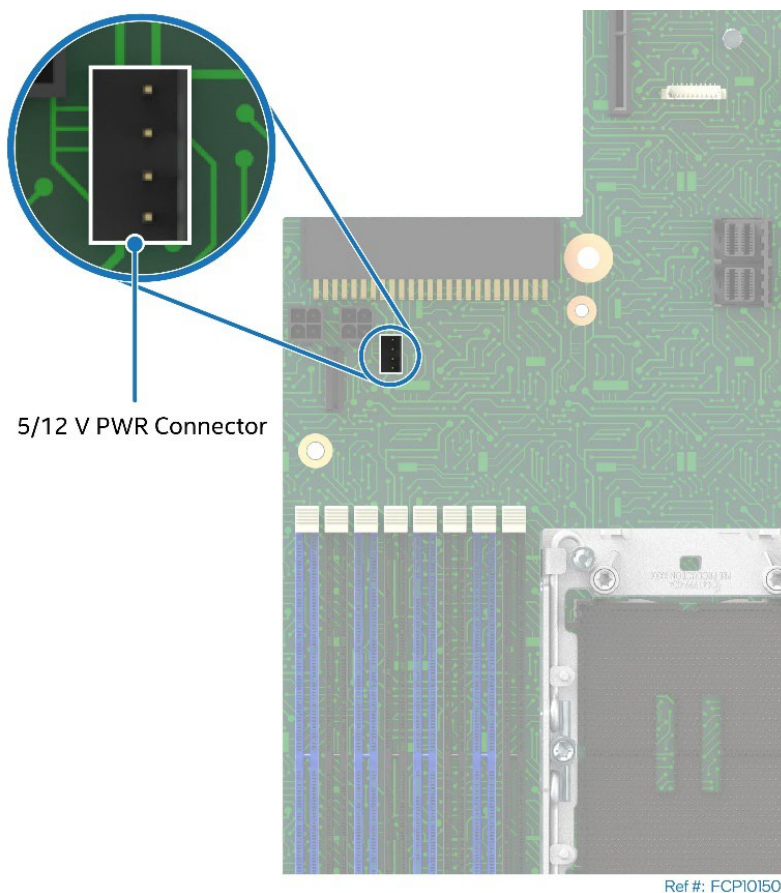
Figure 34. Peripheral Power Connector

The following table provides the pinout for this connector.

Table 17. Peripheral Drive Power Connector Pinout

Pin #	Signal Name
1	P5V
2	GND
3	GND
4	P12V

7.2 Front USB 3.0/2.0 Panel Header and Front Control Panel Header

The server board includes two headers that provide various front panel options. This section provides the pinout for each header. The headers shown in the figure are the same type.
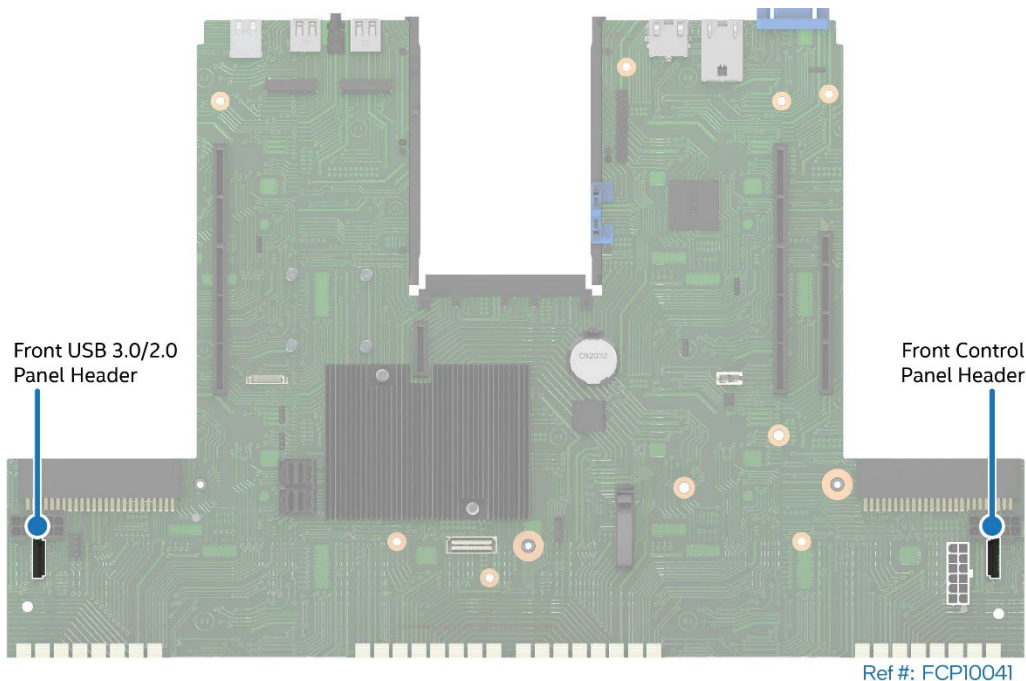
Figure 35. Front Panel Header and Front Control Panel Header

7.2.1 Front USB 3.0/2.0 Panel Header

The Front USB 3.0/2.0 Panel header is 26 pins. The following table provides the pinout.

Table 18. Front USB 3.0/2.0 Panel Header Pinout

Pin #	Signal Name	Pin #	Signal Name
1	P5V_USB3_FP	14	Ground
2	P5V_USB3_FP	15	USB3_BUFF_P01_RXN
3	P5V_USB3_FP	16	USB3_BUFF_P01_RXP
4	P5V_USB3_FP	17	Ground
5	P5V_USB3_FP	18	USB3_BUFF_P01_TXN
6	P5V_USB3_FP	19	USB3_BUFF_P01_TXP
7	P5V_FB_SB	20	Ground
8	Ground	21	USB2_BUFF_P11_DN
9	Ground	22	USB2_BUFF_P11_DP
10	Ground	23	Ground
11	Ground	24	USB2_BUFF_P13_DN
12	Ground	25	USB2_BUFF_P13_DP
13	Ground	26	Ground

7.2.2   Front Control Panel Header Pinout

The Front Control Panel header is 26 pins. The following table provides the pinout.

Table 19. Front Control Panel Header Pinout

Pin #	Signal Name	Pin #	Signal Name
1	GND	14	GND
2	GND	15	NIC1_SPEED_LED _N
3	NIC2_LINK_ACT_LED _N	16	PWR_BTN_N
4	NIC2_SPEED_LED _N	17	HDD_ACT_N
5	NMI_BTN_N	18	STATUS_LED_A_N
6	SPARE	19	STATUS_LED_G_N
7	CHASSIS_INTRUSSION	20	P3V3
8	ID_BTN_N	21	ID_LED_N
9	GND	22	PWR_LED_N
10	SMB_SCL	23	P5V_AUX
11	SMB_SDA	24	SPARE
12	RST_BTN_N	25	P3V3_AUX
13	NIC1_LINK_ACT_LED_N	26	P3V3_AUX

7.3   I²C Connectors

The server board includes two I²C connectors. The header locations are shown in Figure 36 and the pinout is provided in Table 20.

Ref #: FCP10050
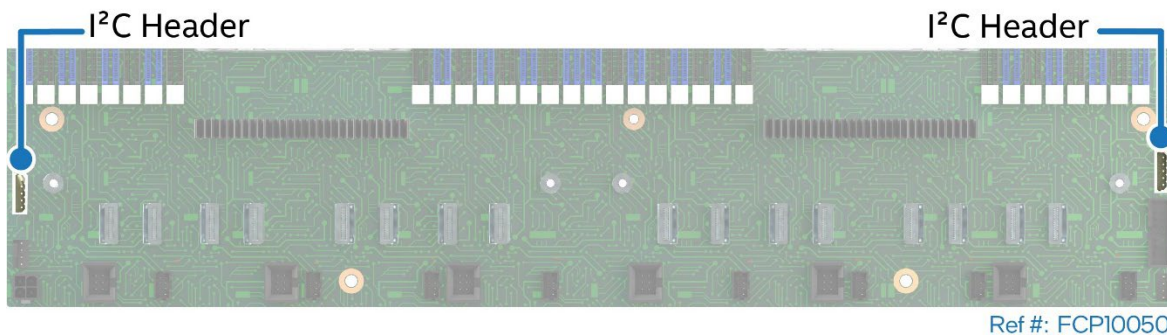
Figure 36. I²C Connectors

Table 20. I²C Cable Connector Pinout

Pin #	Signal Name
1	SMB_3V3_DAT
2	GND
3	SMB_3V3_CLK
4	SMB_ADD0
5	SMB_ADD1

7.4 Fan Connectors

This section provides pinouts for the system fan connectors and CPU fan connectors.

7.4.1 System Fan Connectors

Note: The server board includes a set of eight 8-Pin managed system fan connectors and a set of six 6-pin managed system fan connectors. Concurrent use of all fourteen system fan connectors or using a mix of fan connector types within a given system configuration is not supported. To implement managed system fans, monitored and controlled by server management, system architects must utilize system fan connectors that are of the same type (6-pin or 8-pin).

The Intel® Server Board M50FCP2SBSTD includes eight managed 8-pin fan connectors labeled SYS_FAN #, where # is 1 through 8. The following figure and table show the pinout of these connectors. The maximum power drawn by each 8-pin fan connector is 70 W.
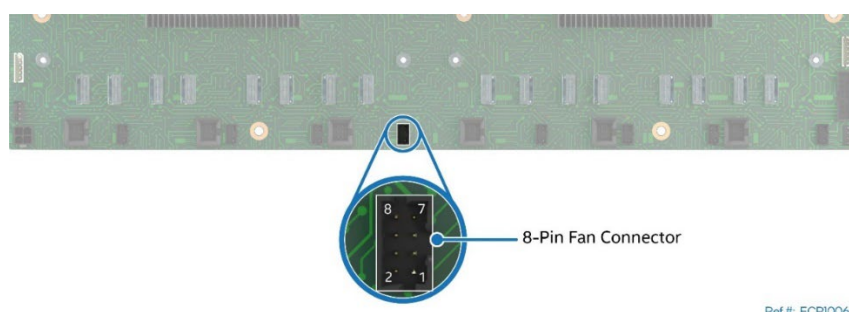
Figure 37. 8-Pin Fan Connector – Intel® Server Board M50FCP2SBSTD

Table 21. 8-Pin Fan Connector Pinout – Intel® Server Board M50FCP2SBSTD

Pin #	Signal Name	Pin #	Signal Name
8	FAN PRSNT	7	GROUND
6	GROUND	5	Fan Tachometer 1 (Sense)
4	P12V FAN	3	P12V FAN
2	FAN PWM	1	Fan Tachometer 2 (Sense)

In addition to the 8-pinn fan connectors shown in Figure 37, the server board also includes six 6-pin managed fan connectors labeled "SYS_FAN #", where # is 1 through 6. The following figure and table show the pinout of the 6-pin fan connector. The maximum power drawn by each 6-pin fan connector is 50.4 W.
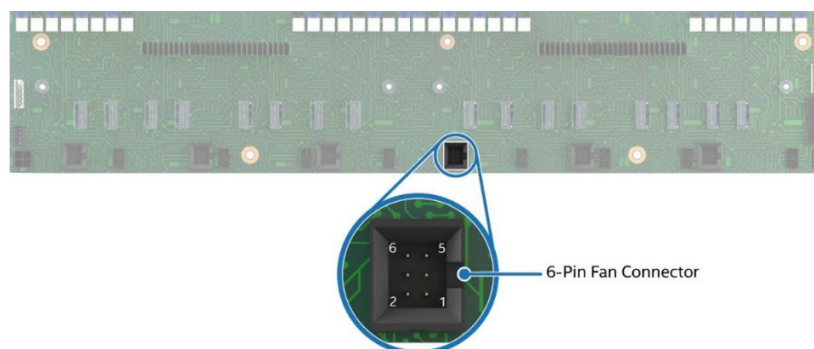
Figure 38. 6-Pin Fan Connector – Intel® Server Board M50FCP2SBSTD

Table 22. 6-Pin Fan Pinout – Intel® Server Board M50FCP2SBSTD

Pin #	Signal Name	Pin #	Signal Name
6	LED FAN FAULT	5	SYS FAN PRSNT
4	FAN PWM	3	FAN TACH
2	P12V FAN	1	GROUND

7.4.2   CPU Fan Connectors

The server board includes two 4-pin managed CPU fan connectors: one for CPU 0 and one for CPU 1.

CPU 0 Fan Connector   CPU 1 Fan Connector

Ref #: FCP10080
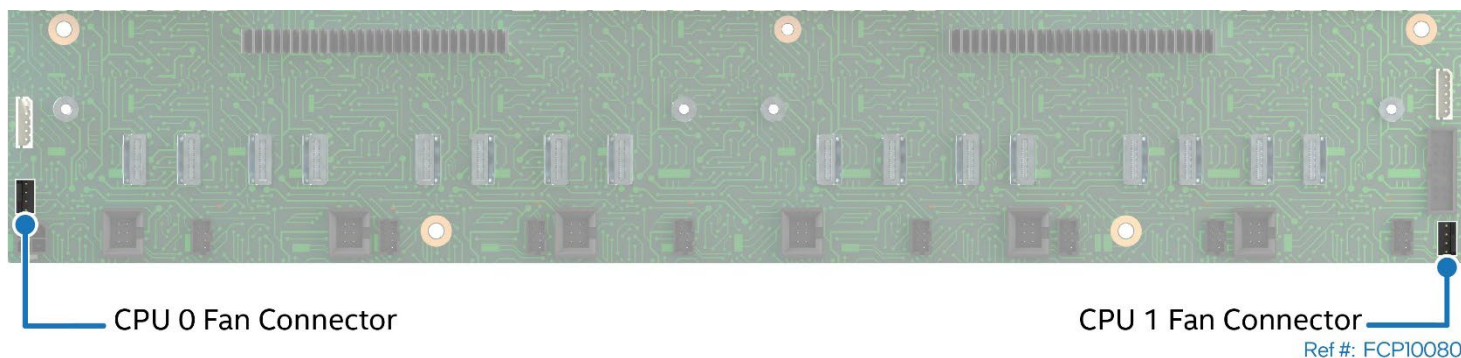
Figure 39. CPU 0 / CPU 1 Fan Connectors

Table 23. CPU 0 / CPU 1 Fan Pinout

Pin #	Signal Name
1	GND
2	12V
3	Tach/Sense
4	PWM (Control)

7.5   PCIe* Mini Cool Edge IO (MCIO*) Connector

To support PCIe NVMe SSDs, the server board includes 16 PCIe 38-pin MCIO* connectors. PCIe lanes from each processor are routed to a bank of eight connectors labeled "CPU 0 PCIe Ports 3A, 3B, 3C, 3D, 4D, 4C, 4B, 4A" and "CPU 1 PCIe Ports 3A, 3B, 3C, 3D, 4D, 4C, 4B, 4A". Each MCIO connector supports x4 PCIe lanes.

Ref #: FCP10091
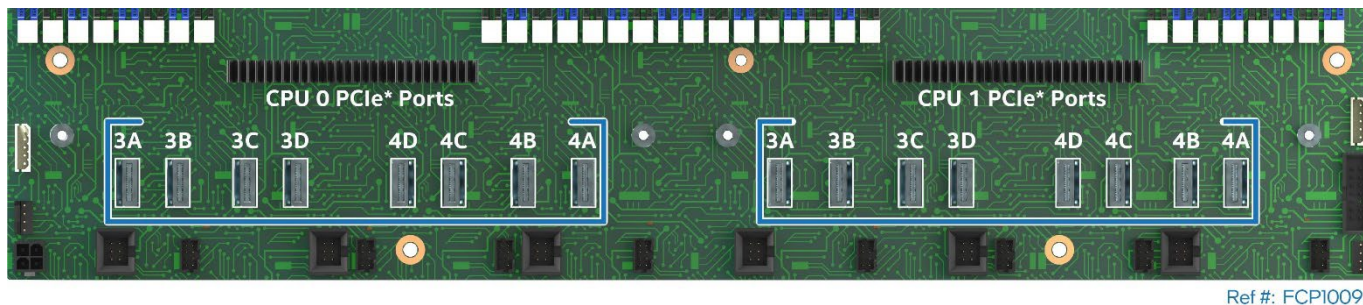
Figure 40. PCIe* MCIO Connectors

The following tables provide the pinout for each PCIe MCIO connector.

Table 24. PCIe* MCIO Connector 3A Pinout (CPU 0 and CPU 1)

MCIO / J8		
Pin number	Pin name	Net name
A1	GND	GND
A2	RX_DP<0>	P4E_CPU0_PE3_NVME_RX_DP<0>
A3	RX_DN<0>	P4E_CPU0_PE3_NVME_RX_DN<0>
A4	GND	GND
A5	RX_DP<1>	P4E_CPU0_PE3_NVME_RX_DP<1>
A6	RX_DN<1>	P4E_CPU0_PE3_NVME_RX_DN<1>
A7	GND	GND
A8	SB7	FM_ROC_CPU0_BIF0
A9	SB3	FM_SSD_CPU0_ID0
A10	GND	GND
A11	SB4	CLK_100M_DB2000_CPU0_NVME8_DP
A12	SB5	CLK_100M_DB2000_CPU0_NVME8_DN
A13	GND	GND
A14	RX_DN<2>	P4E_CPU0_PE3_NVME_RX_DN<2>
A15	RX_DP<2>	P4E_CPU0_PE3_NVME_RX_DP<2>
A16	GND	GND
A17	RX_DP<3>	P4E_CPU0_PE3_NVME_RX_DP<3>
A18	RX_DN<3>	P4E_CPU0_PE3_NVME_RX_DN<3>
A19	GND	GND
B1	GND	GND
B2	TX_DN<0>	P4E_CPU0_PE3_NVME_TX_C_DN<0>
B3	TX_DP<0>	P4E_CPU0_PE3_NVME_TX_C_DP<0>
B4	GND	GND
B5	TX_DP<1>	P4E_CPU0_PE3_NVME_TX_C_DP<1>
B6	TX_DN<1>	P4E_CPU0_PE3_NVME_TX_C_DN<1>
B7	GND	GND
B8	SB0	SMB_PEHPCPU0_NVME_LVC3_SCL
B9	SB1	SMB_PEHPCPU0_NVME_LVC3_SDA
B10	GND	GND
B11	SB2	RST_NVME1_CPU0_PERST_N
B12	SB6	FM_NVME1_CPU0_PRSTN_N
B13	GND	GND
B14	TX_DP<2>	P4E_CPU0_PE3_NVME_TX_C_DP<2>
B15	TX_DN<2>	P4E_CPU0_PE3_NVME_TX_C_DN<2>
B16	GND	GND
B17	TX_DP<3>	P4E_CPU0_PE3_NVME_TX_C_DP<3>
B18	TX_DN<3>	P4E_CPU0_PE3_NVME_TX_C_DN<3>
B19	GND	GND

Table 25. PCIe* MCIO Connector 3B Pinout (CPU 0 and CPU 1)

MCIO / J64		
Pin number	Pin name	Net name
A1	GND	GND
A2	RX_DP<0>	P4E_CPU0_PE3_NVME_RX_DP<4>
A3	RX_DN<0>	P4E_CPU0_PE3_NVME_RX_DN<4>
A4	GND	GND
A5	RX_DP<1>	P4E_CPU0_PE3_NVME_RX_DN<5>
A6	RX_DN<1>	P4E_CPU0_PE3_NVME_RX_DP<5>
A7	GND	GND
A8	SB7	TP_CPU0_NVME2_SPARE_A8
A9	SB3	FM_SSD_CPU0_ID1
A10	GND	GND
A11	SB4	CLK_100M_DB2000_CPU0_NVME7_DP
A12	SB5	CLK_100M_DB2000_CPU0_NVME7_DN
A13	GND	GND
A14	RX_DN<2>	P4E_CPU0_PE3_NVME_RX_DP<6>
A15	RX_DP<2>	P4E_CPU0_PE3_NVME_RX_DN<6>
A16	GND	GND
A17	RX_DP<3>	P4E_CPU0_PE3_NVME_RX_DP<7>
A18	RX_DN<3>	P4E_CPU0_PE3_NVME_RX_DN<7>
A19	GND	GND
B1	GND	GND
B2	TX_DN<0>	P4E_CPU0_PE3_NVME_TX_C_DP<4>
B3	TX_DP<0>	P4E_CPU0_PE3_NVME_TX_C_DN<4>
B4	GND	GND
B5	TX_DP<1>	P4E_CPU0_PE3_NVME_TX_C_DP<5>
B6	TX_DN<1>	P4E_CPU0_PE3_NVME_TX_C_DN<5>
B7	GND	GND
B8	SB0	FM_SMB_CPU0_NVME_ALERT_N
B9	SB1	TP_NVME2_CPU0_B9
B10	GND	GND
B11	SB2	RST_NVME2_CPU0_PERST_N
B12	SB6	FM_NVME2_CPU0_PRSTN_N
B13	GND	GND
B14	TX_DP<2>	P4E_CPU0_PE3_NVME_TX_C_DP<6>
B15	TX_DN<2>	P4E_CPU0_PE3_NVME_TX_C_DN<6>
B16	GND	GND
B17	TX_DP<3>	P4E_CPU0_PE3_NVME_TX_C_DP<7>
B18	TX_DN<3>	P4E_CPU0_PE3_NVME_TX_C_DN<7>
B19	GND	GND

Table 26. PCIe* MCIO Connector 3C Pinout (CPU 0 and CPU 1)

MCIO / J30		
Pin number	Pin name	Net name
A1	GND	GND
A2	RX_DP<0>	P4E_CPU0_PE3_NVME_RX_DN<8>
A3	RX_DN<0>	P4E_CPU0_PE3_NVME_RX_DP<8>
A4	GND	GND
A5	RX_DP<1>	P4E_CPU0_PE3_NVME_RX_DP<9>
A6	RX_DN<1>	P4E_CPU0_PE3_NVME_RX_DN<9>
A7	GND	GND
A8	SB7	FM_ROC_CPU0_BIF1
A9	SB3	FM_SSD_CPU0_ID2
A10	GND	GND
A11	SB4	CLK_100M_DB2000_CPU0_NVME6_DP
A12	SB5	CLK_100M_DB2000_CPU0_NVME6_DN
A13	GND	GND
A14	RX_DN<2>	P4E_CPU0_PE3_NVME_RX_DN<10>
A15	RX_DP<2>	P4E_CPU0_PE3_NVME_RX_DP<10>
A16	GND	GND
A17	RX_DP<3>	P4E_CPU0_PE3_NVME_RX_DP<11>
A18	RX_DN<3>	P4E_CPU0_PE3_NVME_RX_DN<11>
A19	GND	GND
B1	GND	GND
B2	TX_DN<0>	P4E_CPU0_PE3_NVME_TX_C_DP<8>
B3	TX_DP<0>	P4E_CPU0_PE3_NVME_TX_C_DN<8>
B4	GND	GND
B5	TX_DP<1>	P4E_CPU0_PE3_NVME_TX_C_DP<9>
B6	TX_DN<1>	P4E_CPU0_PE3_NVME_TX_C_DN<9>
B7	GND	GND
B8	SB0	SMB_PEHPCPU0_NVME_LVC3_SCL
B9	SB1	SMB_PEHPCPU0_NVME_LVC3_SDA
B10	GND	GND
B11	SB2	RST_NVME3_CPU0_PERST_N
B12	SB6	FM_NVME3_CPU0_PRSTN_N
B13	GND	GND
B14	TX_DP<2>	P4E_CPU0_PE3_NVME_TX_C_DP<10>
B15	TX_DN<2>	P4E_CPU0_PE3_NVME_TX_C_DN<10>
B16	GND	GND
B17	TX_DP<3>	P4E_CPU0_PE3_NVME_TX_C_DP<11>
B18	TX_DN<3>	P4E_CPU0_PE3_NVME_TX_C_DN<11>
B19	GND	GND

Table 27. PCIe* MCIO Connector 3D Pinout (CPU 0 and CPU 1)

MCIO / J63		
Pin number	Pin name	Net name
A1	GND	GND
A2	RX_DP<0>	P4E_CPU0_PE3_NVME_RX_DP<12>
A3	RX_DN<0>	P4E_CPU0_PE3_NVME_RX_DN<12>
A4	GND	GND
A5	RX_DP<1>	P4E_CPU0_PE3_NVME_RX_DN<13>
A6	RX_DN<1>	P4E_CPU0_PE3_NVME_RX_DP<13>
A7	GND	GND
A8	SB7	TP_CPU0_NVME4_SPARE_A8
A9	SB3	FM_SSD_CPU0_ID3
A10	GND	GND
A11	SB4	CLK_100M_DB2000_CPU0_NVME5_DP
A12	SB5	CLK_100M_DB2000_CPU0_NVME5_DN
A13	GND	GND
A14	RX_DN<2>	P4E_CPU0_PE3_NVME_RX_DP<14>
A15	RX_DP<2>	P4E_CPU0_PE3_NVME_RX_DN<14>
A16	GND	GND
A17	RX_DP<3>	P4E_CPU0_PE3_NVME_RX_DP<15>
A18	RX_DN<3>	P4E_CPU0_PE3_NVME_RX_DN<15>
A19	GND	GND
B1	GND	GND
B2	TX_DN<0>	P4E_CPU0_PE3_NVME_TX_C_DP<12>
B3	TX_DP<0>	P4E_CPU0_PE3_NVME_TX_C_DN<12>
B4	GND	GND
B5	TX_DP<1>	P4E_CPU0_PE3_NVME_TX_C_DP<13>
B6	TX_DN<1>	P4E_CPU0_PE3_NVME_TX_C_DN<13>
B7	GND	GND
B8	SB0	FM_SMB_CPU0_NVME_ALERT_N
B9	SB1	TP_NVME4_CPU0_B9
B10	GND	GND
B11	SB2	RST_NVME4_CPU0_PERST_N
B12	SB6	FM_NVME4_CPU0_PRSTN_N
B13	GND	GND
B14	TX_DP<2>	P4E_CPU0_PE3_NVME_TX_C_DP<14>
B15	TX_DN<2>	P4E_CPU0_PE3_NVME_TX_C_DN<14>
B16	GND	GND
B17	TX_DP<3>	P4E_CPU0_PE3_NVME_TX_C_DP<15>
B18	TX_DN<3>	P4E_CPU0_PE3_NVME_TX_C_DN<15>
B19	GND	GND

Table 28. PCIe* MCIO Connector 4D Pinout (CPU 0 and CPU 1)

MCIO / J71		
Pin number	Pin name	Net name
A1	GND	GND
A2	RX_DP<0>	P4E_CPU0_PE4_NVME_RX_DP<12>
A3	RX_DN<0>	P4E_CPU0_PE4_NVME_RX_DN<12>
A4	GND	GND
A5	RX_DP<1>	P4E_CPU0_PE4_NVME_RX_DP<13>
A6	RX_DN<1>	P4E_CPU0_PE4_NVME_RX_DN<13>
A7	GND	GND
A8	SB7	TP_CPU1_NVME2_SPARE_A8
A9	SB3	FM_SSD_CPU1_ID1
A10	GND	GND
A11	SB4	CLK_100M_DB2000_CPU0_NVME4_DP
A12	SB5	CLK_100M_DB2000_CPU0_NVME4_DN
A13	GND	GND
A14	RX_DN<2>	P4E_CPU0_PE4_NVME_RX_DP<14>
A15	RX_DP<2>	P4E_CPU0_PE4_NVME_RX_DN<14>
A16	GND	GND
A17	RX_DP<3>	P4E_CPU0_PE4_NVME_RX_DP<15>
A18	RX_DN<3>	P4E_CPU0_PE4_NVME_RX_DN<15>
A19	GND	GND
B1	GND	GND
B2	TX_DN<0>	P4E_CPU0_PE4_NVME_TX_C_DP<12>
B3	TX_DP<0>	P4E_CPU0_PE4_NVME_TX_C_DN<12>
B4	GND	GND
B5	TX_DP<1>	P4E_CPU0_PE4_NVME_TX_C_DP<13>
B6	TX_DN<1>	P4E_CPU0_PE4_NVME_TX_C_DN<13>
B7	GND	GND
B8	SB0	FM_SMB_CPU1_NVME_ALERT_N
B9	SB1	TP_NVME2_CPU1_B9
B10	GND	GND
B11	SB2	RST_NVME8_CPU0_PERST_N
B12	SB6	FM_NVME8_CPU0_PRSTN_N
B13	GND	GND
B14	TX_DP<2>	P4E_CPU0_PE4_NVME_TX_C_DP<14>
B15	TX_DN<2>	P4E_CPU0_PE4_NVME_TX_C_DN<14>
B16	GND	GND
B17	TX_DP<3>	P4E_CPU0_PE4_NVME_TX_C_DP<15>
B18	TX_DN<3>	P4E_CPU0_PE4_NVME_TX_C_DN<15>
B19	GND	GND

Table 29. PCIe* MCIO Connector 4C Pinout (CPU 0 and CPU 1)

MCIO / J70		
Pin number	Pin name	Net name
A1	GND	GND
A2	RX_DP<0>	P4E_CPU0_PE4_NVME_RX_DP<8>
A3	RX_DN<0>	P4E_CPU0_PE4_NVME_RX_DN<8>
A4	GND	GND
A5	RX_DP<1>	P4E_CPU0_PE4_NVME_RX_DP<9>
A6	RX_DN<1>	P4E_CPU0_PE4_NVME_RX_DN<9>
A7	GND	GND
A8	SB7	TP_CPU0_NVME7_SPARE_A8
A9	SB3	FM_SSD_CPU0_ID6
A10	GND	GND
A11	SB4	CLK_100M_DB2000_CPU0_NVME3_DP
A12	SB5	CLK_100M_DB2000_CPU0_NVME3_DN
A13	GND	GND
A14	RX_DN<2>	P4E_CPU0_PE4_NVME_RX_DP<10>
A15	RX_DP<2>	P4E_CPU0_PE4_NVME_RX_DN<10>
A16	GND	GND
A17	RX_DP<3>	P4E_CPU0_PE4_NVME_RX_DP<11>
A18	RX_DN<3>	P4E_CPU0_PE4_NVME_RX_DN<11>
A19	GND	GND
B1	GND	GND
B2	TX_DN<0>	P4E_CPU0_PE4_NVME_TX_C_DP<8>
B3	TX_DP<0>	P4E_CPU0_PE4_NVME_TX_C_DN<8>
B4	GND	GND
B5	TX_DP<1>	P4E_CPU0_PE4_NVME_TX_C_DP<9>
B6	TX_DN<1>	P4E_CPU0_PE4_NVME_TX_C_DN<9>
B7	GND	GND
B8	SB0	SMB_PEHPCPU0_NVME_LVC3_SCL
B9	SB1	SMB_PEHPCPU0_NVME_LVC3_SDA
B10	GND	GND
B11	SB2	RST_NVME7_CPU0_PERST_N
B12	SB6	FM_NVME7_CPU0_PRSTN_N
B13	GND	GND
B14	TX_DP<2>	P4E_CPU0_PE4_NVME_TX_C_DP<10>
B15	TX_DN<2>	P4E_CPU0_PE4_NVME_TX_C_DN<10>
B16	GND	GND
B17	TX_DP<3>	P4E_CPU0_PE4_NVME_TX_C_DN<11>
B18	TX_DN<3>	P4E_CPU0_PE4_NVME_TX_C_DP<11>
B19	GND	GND

Table 30. PCIe* MCIO Connector 4B Pinout (CPU 0 and CPU 1)

MCIO / J72		
Pin number	Pin name	Net name
A1	GND	GND
A2	RX_DP<0>	P4E_CPU0_PE4_NVME_RX_DP<4>
A3	RX_DN<0>	P4E_CPU0_PE4_NVME_RX_DN<4>
A4	GND	GND
A5	RX_DP<1>	P4E_CPU0_PE4_NVME_RX_DP<5>
A6	RX_DN<1>	P4E_CPU0_PE4_NVME_RX_DN<5>
A7	GND	GND
A8	SB7	TP_CPU0_NVME6_SPARE_A8
A9	SB3	FM_SSD_CPU0_ID5
A10	GND	GND
A11	SB4	CLK_100M_DB2000_CPU0_NVME2_DP
A12	SB5	CLK_100M_DB2000_CPU0_NVME2_DN
A13	GND	GND
A14	RX_DN<2>	P4E_CPU0_PE4_NVME_RX_DP<6>
A15	RX_DP<2>	P4E_CPU0_PE4_NVME_RX_DN<6>
A16	GND	GND
A17	RX_DP<3>	P4E_CPU0_PE4_NVME_RX_DP<7>
A18	RX_DN<3>	P4E_CPU0_PE4_NVME_RX_DN<7>
A19	GND	GND
B1	GND	GND
B2	TX_DN<0>	P4E_CPU0_PE4_NVME_TX_C_DP<4>
B3	TX_DP<0>	P4E_CPU0_PE4_NVME_TX_C_DN<4>
B4	GND	GND
B5	TX_DP<1>	P4E_CPU0_PE4_NVME_TX_C_DP<5>
B6	TX_DN<1>	P4E_CPU0_PE4_NVME_TX_C_DN<5>
B7	GND	GND
B8	SB0	FM_SMB_CPU0_NVME_ALERT_N
B9	SB1	TP_NVME6_CPU0_B9
B10	GND	GND
B11	SB2	RST_NVME6_CPU0_PERST_N
B12	SB6	FM_NVME6_CPU0_PRSTN_N
B13	GND	GND
B14	TX_DP<2>	P4E_CPU0_PE4_NVME_TX_C_DP<6>
B15	TX_DN<2>	P4E_CPU0_PE4_NVME_TX_C_DN<6>
B16	GND	GND
B17	TX_DP<3>	P4E_CPU0_PE4_NVME_TX_C_DP<7>
B18	TX_DN<3>	P4E_CPU0_PE4_NVME_TX_C_DN<7>
B19	GND	GND

Table 31. PCIe* MCIO Connector 4A Pinout (CPU 0 and CPU 1)

MCIO / J69		
Pin number	Pin name	Net name
A1	GND	GND
A2	RX_DP<0>	P4E_CPU0_PE4_NVME_RX_DN<0>
A3	RX_DN<0>	P4E_CPU0_PE4_NVME_RX_DP<0>
A4	GND	GND
A5	RX_DP<1>	P4E_CPU0_PE4_NVME_RX_DP<1>
A6	RX_DN<1>	P4E_CPU0_PE4_NVME_RX_DN<1>
A7	GND	GND
A8	SB7	TP_CPU0_NVME5_SPARE_A8
A9	SB3	FM_SSD_CPU0_ID4
A10	GND	GND
A11	SB4	CLK_100M_DB2000_CPU0_NVME1_DP
A12	SB5	CLK_100M_DB2000_CPU0_NVME1_DN
A13	GND	GND
A14	RX_DN<2>	P4E_CPU0_PE4_NVME_RX_DP<2>
A15	RX_DP<2>	P4E_CPU0_PE4_NVME_RX_DN<2>
A16	GND	GND
A17	RX_DP<3>	P4E_CPU0_PE4_NVME_RX_DP<3>
A18	RX_DN<3>	P4E_CPU0_PE4_NVME_RX_DN<3>
A19	GND	GND
B1	GND	GND
B2	TX_DN<0>	P4E_CPU0_PE4_NVME_TX_C_DP<0>
B3	TX_DP<0>	P4E_CPU0_PE4_NVME_TX_C_DN<0>
B4	GND	GND
B5	TX_DP<1>	P4E_CPU0_PE4_NVME_TX_C_DN<1>
B6	TX_DN<1>	P4E_CPU0_PE4_NVME_TX_C_DP<1>
B7	GND	GND
B8	SB0	SMB_PEHPCPU0_NVME_LVC3_SCL
B9	SB1	SMB_PEHPCPU0_NVME_LVC3_SDA
B10	GND	GND
B11	SB2	RST_NVME5_CPU0_PERST_N
B12	SB6	FM_NVME5_CPU0_PRSTN_N
B13	GND	GND
B14	TX_DP<2>	P4E_CPU0_PE4_NVME_TX_C_DP<2>
B15	TX_DN<2>	P4E_CPU0_PE4_NVME_TX_C_DN<2>
B16	GND	GND
B17	TX_DP<3>	P4E_CPU0_PE4_NVME_TX_C_DP<3>
B18	TX_DN<3>	P4E_CPU0_PE4_NVME_TX_C_DN<3>
B19	GND	GND

8.   PCI Express* (PCIe*) Support

This chapter provides information on the Intel® Server Board M50FCP2SBSTD PCI Express (PCIe) support. The PCIe interfaces supporting riser slots and server board PCIe MCIO connectors are fully compliant with the *PCIe Base Specification, Revision 5.0* supporting the following PCIe bit rates: 5.0 (32 GT/s), 4.0 (16 GT/s), 3.0 (8.0 GT/s), 2.0 (5.0 GT/s), and 1.0 (2.5 GT/s).

The following table provides the processor/chipset port routing for PCIe-based server board connectors including OCP connector, PCIe MCIO connectors, and riser card slots. The interfaces supporting M.2 connectors are fully compliant with the *PCIe Base Specification, Revision 3.0* supporting the following PCIe* bit rates: 3.0 (8.0 GT/s), 2.0 (5.0 GT/s), and 1.0 (2.5 GT/s).

Table 32. Processor / Chipset PCIe* Port Routing

Host	Port	Width	PCIe* Revision	Usage
CPU 0	Port 0A–0D	x16	4.0	OCP* Adapter connector
	Port 1A–1D	x16	5.0	Riser Slot #1 [15:0]
	Port 2A–2D	x16	5.0	Riser Slot #1 [31:16]
	Port 3A–3D	x16	5.0	Server board PCIe* MCIO connectors
	Port 4A–4D	x16	5.0	Server board PCIe* MCIO connectors
	DMI3	x8	3.0	Chipset PCH
CPU 1	Port 0A–0D	x16	5.0	Riser Slot #3 [15:0]
	Port 1A–1D	x16	5.0	Riser Slot #2 [31:16]
	Port 2A–2D	x16	5.0	Riser Slot #2 [15:0]
	Port 3A–3D	x16	5.0	Server board PCIe* MCIO connectors
	Port 4A–4D	x16	5.0	Server board PCIe* MCIO connectors
Chipset PCH	Port 4–7	x2	3.0	M.2 Connector- SATA / PCIe*
	Port 8–11	x2	3.0	M.2 Connector- SATA / PCIe*

8.1   PCIe* Enumeration and Allocation

The BIOS assigns PCIe bus numbers in a depth-first hierarchy, in accordance with the *PCIe* Base Specification, Revision 5.0*. The bus number is incremented when the BIOS encounters a PCI-PCI bridge device.

Scanning continues with the secondary side of the bridge until all subordinate buses are assigned numbers. PCIe bus number assignments may vary from boot to boot with varying presence of PCI devices with PCI-PCI bridges.

If a bridge device with a single bus behind it is inserted into a PCIe bus, all subsequent PCIe bus numbers below the current bus are increased by one. The bus assignments occur once, early in the BIOS boot process, and never change during the pre-boot phase.

8.2   PCIe* Riser Card Support

The server board includes riser card slots identified as Riser Slot #1, Riser Slot #2, Riser Slot #3, and Interposer Riser Slot. The PCIe data lanes for Riser Slot #1 are routed from CPU 0. The PCIe data lanes for Riser Slot #2, Riser Slot #3, and the Interposer Riser Slot are routed from CPU 1. Riser Slots #2 & #3, and the Interposer Riser Slot are only supported in dual processor configurations.

Notes:
- The riser card slots are specifically designed to support riser cards only. Attempting to install a PCIe add-in card directly into a riser card slot on the server board may damage the server board, the add-in card, or both.
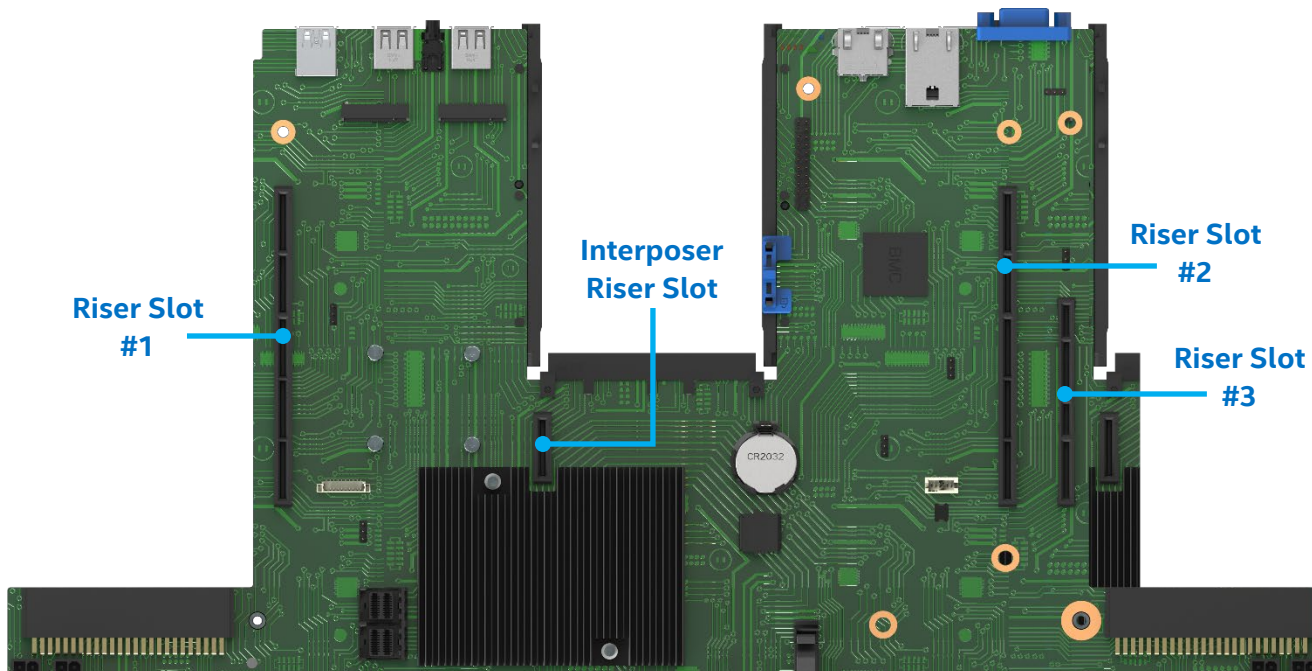
Figure 41. Riser Card Slots

Intel offers several PCIe riser card accessory options for this server board. The following sections provide information for each option.

The available riser card options are riser slot specific and are not interchangeable between the server board riser slots.

- Add-in cards connected to the riser card in Riser Slot #1 must be oriented with component side up.
- Add-in cards connected to the riser card in Riser Slot #2 must be oriented with component side down.
- Add-in cards connected to the riser card in Riser Slot #3 must be oriented with component side up.

In the following sections, FH = Full Height, FL = Full Length, HL =Half Length, LP = Low Profile.

8.2.1   2U Three-Slot PCIe* Riser Card for Riser Slot #1 (iPC FCP2URISER1STD)

This three-slot PCIe riser card option supports:

- One FH/FL single-width add-in card slot (x16 electrical, x16 mechanical)
- One FH/FL single-width add-in card slot (x8 electrical, x16 mechanical)
- One FH/HL single-width add-in card slot (x8 electrical, x8 mechanical)
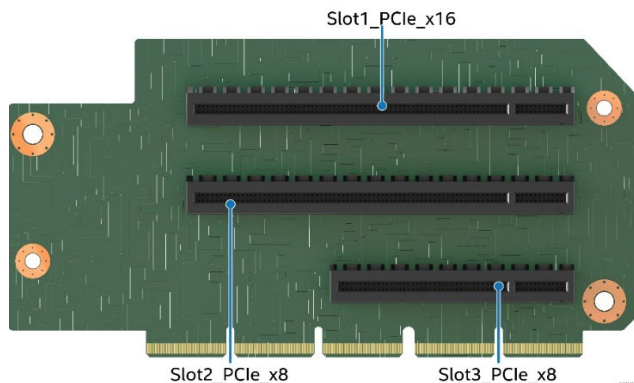
Figure 42. PCIe* Riser Card for Riser Slot #1

Table 33. PCIe* Riser Card Connector Description

Connector	Description	Maximum Available Power (W)
Slot1_PCIe_x16	CPU 0 – Ports 2A through 2D (x16 electrical, x16 mechanical)	75
Slot2_PCIe_x8	CPU 0 – Ports 1A and 1B (x8 electrical, x16 mechanical)	50
Slot3_PCIe_x8	CPU 0 – Ports 1C and 1D (x8 electrical, x8 mechanical)	25

8.2.2   2U Two-Slot PCIe* Riser Card for Riser Slot #1 (iPC FCP2URISER1DW)

This two-slot PCIe riser card option supports:

- One FH/FL double-width slot (x16 electrical, x16 mechanical)
- One FH/HL single-width slot (x16 electrical, x16 mechanical)

Note: Support for high-power double-width add-in cards requires the system configuration to include the use of a 1U CPU heat sink and GPGPU air duct.
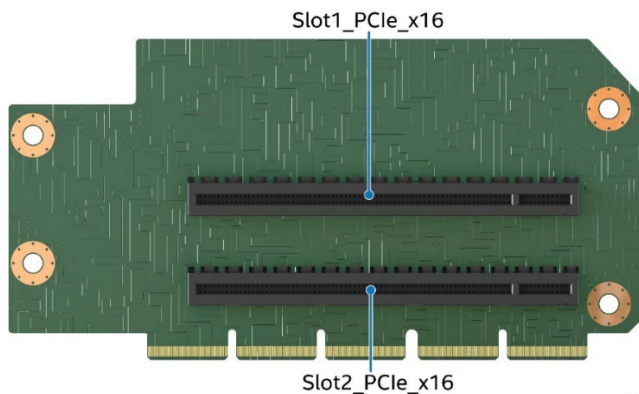
Figure 43. Two-Slot PCIe* Riser Card for Riser Slot #1

Table 34. Two-slot PCIe* Riser Card Connector Description

Connector	Description	Maximum Available Power (W)
Slot1_PCIe_x16	CPU 0 – Ports 2A through 2D (x16 electrical, x16 mechanical)	75
Slot2_PCIe_x16	CPU 0 – Ports 1A through 1D (x16 electrical, x16 mechanical)	75

8.2.3   2U Two-Slot PCIe* Riser Card for Riser Slot #1 (iPC FCP2URISER1SW)

This two-slot PCIe riser card option supports:

- Two FH/FL single-width slot (x16 electrical, x16 mechanical)
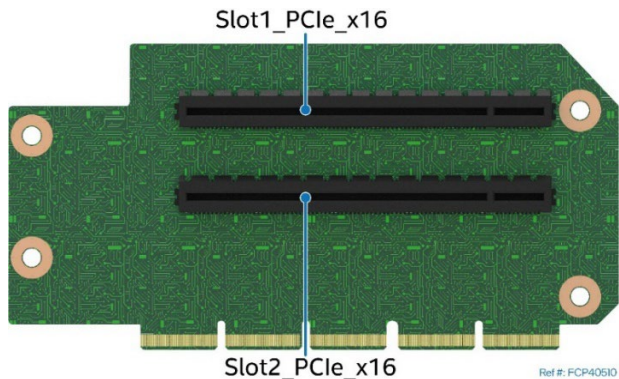
Figure 44. Two-Slot PCIe* Riser Card for Riser Slot #1

Table 35. Two-slot PCIe* Riser Card Connector Description

Connector	Description	Maximum Available Power (W)
Slot1_PCIe_x16	CPU 0 – Ports 2A through 2D (x16 electrical, x16 mechanical)	75
Slot2_PCIe_x16	CPU 0 – Ports 1A through 1D (x16 electrical, x16 mechanical)	75

8.2.4   2U PCIe* NVMe* Riser Card for Riser Slot #1 (iPC FCP2URISER1RTM)

The PCIe NVMe riser card option supports:

- One HL or FL single-width slot (x16 electrical, x16 mechanical)
- Two x8 PCIe NVMe MCIO connectors
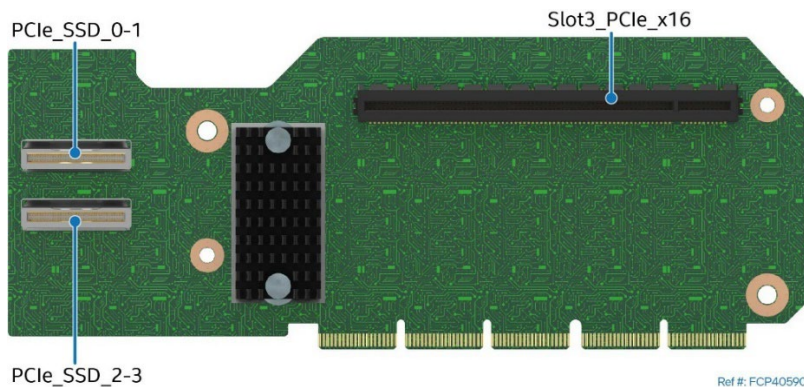
Figure 45. PCIe* NVMe* Riser Card for Riser Slot #1

Table 36. PCIe* NVMe* Riser Card Connector Description

Connector	Description	Maximum Available Power (W)
Slot3_PCIe_x16	CPU 0 – Ports 1A through 1B (x16 electrical, x16 mechanical)	75
PCIe_SSD_0-1	CPU 0 – Ports 2A through 2B (x8 electrical, x8 mechanical)	N/A
PCIe_SSD_2-3	CPU 0 – Ports 2C through 2D (x8 electrical, x8 mechanical)	N/A

8.2.5   2U Three–Slot PCIe* Riser Card for Riser Slot #2 (iPC FCP2URISER2STD)

This three-slot PCIe riser card option supports:

- One FH/FL single-width slot (x16 electrical, x16 mechanical)
- One FH/FL single-width slot (x8 electrical, x16 mechanical)
- One FH/HL single-width slot (x8 electrical, x8 mechanical)
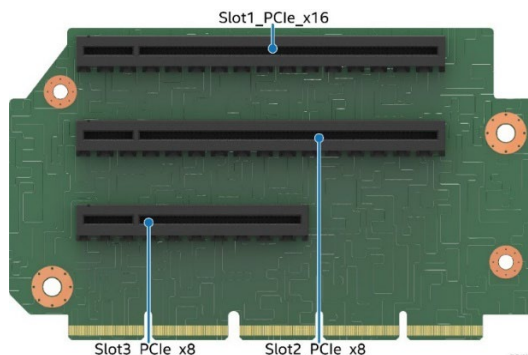
Figure 46. Three-slot PCIe* Riser Card for Riser Slot #2

Table 37. Three–Slot PCIe* Riser Card Connector Description

Connector	Description	Maximum Available Power (W)
Slot1_PCIe_x16	CPU 1 – Ports 1A through 1D (x16 electrical, x16 mechanical)	75
Slot2_PCIe_x8	CPU 1 – Ports 2A and 2B (x8 electrical, x16 mechanical)	50
Slot3_PCIe_x8	CPU 1 – Ports 2C and 2D (x8 electrical, x8 mechanical)	25

8.2.6   2U Two-Slot PCIe* Riser Card for Riser Slot #2 (iPC FCP2URISER2DW)

The two-slot PCIe riser card option supports:

- One FH/FL double-width slot (x16 electrical, x16 mechanical)
- One FH/HL single-width slot (x16 electrical, x16 mechanical)
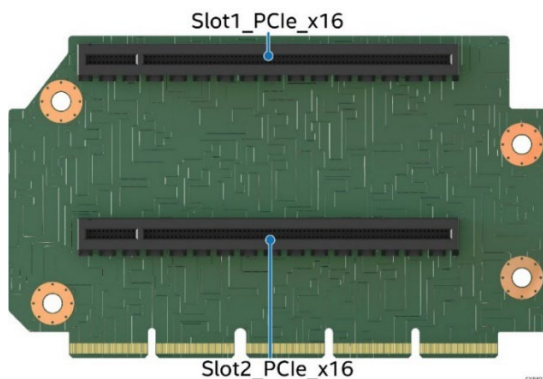
Figure 47. Two-slot PCIe* Riser Card for Riser Slot #2

Table 38. Two–Slot PCIe* Riser Card Connector Description

Connector	Description	Maximum Available Power (W)
Slot1_PCIe_x16	CPU 1 – Ports 1A through 1D (x16 electrical, x16 mechanical)	75
Slot2_PCIe_x16	CPU 1 – Ports 2A through 2D (x16 electrical, x16 mechanical)	75

8.2.7 2U Two-Slot PCIe* Riser Card for Riser Slot #2 (iPC FCP2URISER2SW)

This two-slot PCIe riser card option supports:

- Two FH/FL single-width slots (x16 electrical, x16 mechanical)
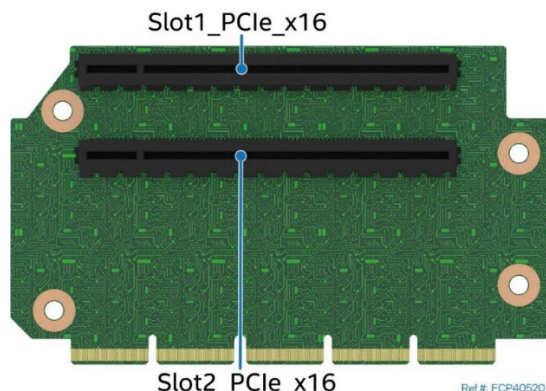
Figure 48. Two-slot PCIe* Riser Card for Riser Slot #2

Table 39. Two-slot PCIe* Riser Card Connector Description

Connector	Description	Maximum Available Power (W)
Slot1_PCIe_x16	CPU 1 – Ports 1A through 1D (x16 electrical, x16 mechanical)	75
Slot2_PCIe_x16	CPU 1 – Ports 2A through 2D (x16 electrical, x16 mechanical)	75

8.2.8 2U Two-Slot PCIe* Riser Card for Riser Slot #3 (iPC FCP2URISER3STD)

This two slot PCIe riser card option supports:

- Two LP/HL single-width slots (x8 electrical, x16 mechanical)
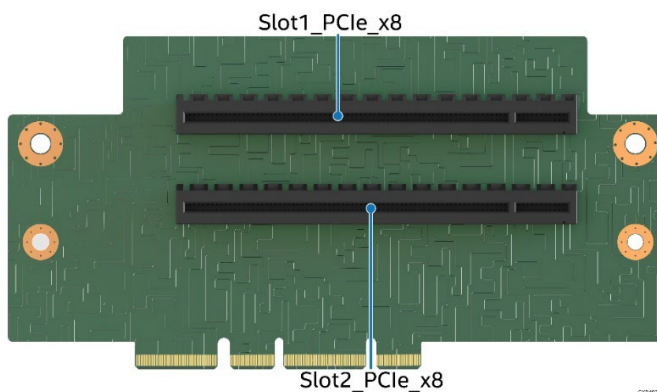
Figure 49. Two-slot PCIe* Riser Card for Riser Slot #3

Table 40. Two-slot PCIe* Riser Card Connector Description

Connector	Description	Maximum Available Power (W)
Slot1_PCIe_x8	CPU 1 – Ports 0A and 0B (X8 electrical, x16 mechanical)	40
Slot2_PCIe_x8	CPU 1 – Ports 0C and 0D (X8 electrical, x16 mechanical)	40

8.2.9   1U One-Slot PCIe* Riser Card for Riser Slot #1 (iPC FCP1URISER1)

This one-slot PCIe riser card option supports:

- One LP/HL, add-in card slot (x16 electrical, x16 mechanical)
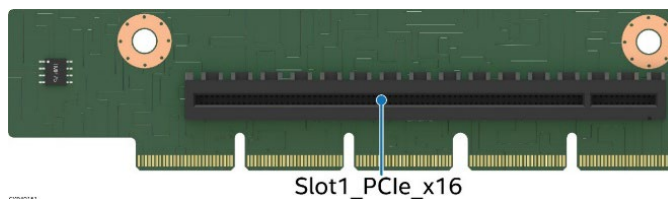
Figure 50. PCIe* Riser Card for Riser Slot #1

Table 41. PCIe* Riser Card Connector Description

Connectors	Description	Maximum Available Power (W)
Slot1_PCIe_x16	CPU 0: Ports 2A through 2D (x16 electrical, x16 mechanical)	75

8.2.10   1U One-Slot PCIe* Riser Card for Riser Slot #2 (iPC FCP1URISER2)

This one-slot PCIe riser card option supports:

- One LP/HL, add-in card slot (x16 electrical, x16 mechanical)
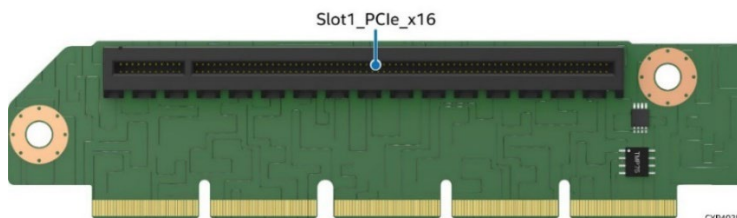
Figure 51. PCIe* Riser Card for Riser Slot #2

Table 42. PCIe* Riser Card Connector Description

Connector	Description	Maximum Available Power (W)
Slot1_PCIe_x16	CPU 1: Ports 1A through 1D (x16 electrical, x16 mechanical)	75

8.2.11   1U PCIe* MCIO Riser Card for Riser Slot #2 with PCIe Interposer Riser Card Support

Intel offers a 1U riser card accessory kit (**iPC – FCP1URISER2KIT**) that provides the server board with the option of adding a third PCIe add-in card into a 1U server system. The kit includes the following:

- 1 – PCIe MCIO riser card for Riser Slot #2
- 1 – PCIe interposer riser card
- 1 – PCIe interposer cable

The PCIe MCIO riser card is only supported when installed into Riser Slot #2 on the server board. The riser card supports the following features:

- One LP/HL add-in card slot (x16 electrical, x16 mechanical)
- One x8 PCIe MCIO* Interposer Cable Connector

Note: The MCIO* Interposer cable connector on the PCIe MCIO Riser card does not support and cannot be used to provide PCIe signals to NVMe drives.
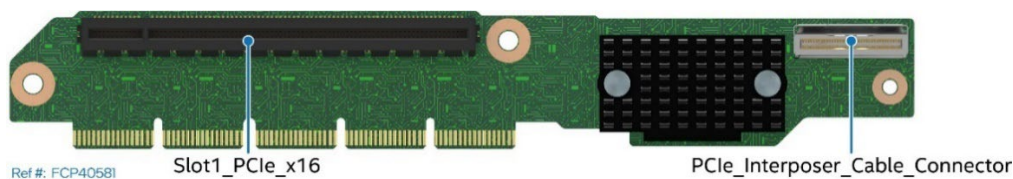
Figure 52. PCIe* Riser Card for Riser Slot #2

Table 43. PCIe* Riser Card Connector Description

Connector	Description	Maximum Available Power (W)
Slot1_PCIe_x16	CPU 1: Ports 2A through 2D (x16 electrical, x16 mechanical)	75
PCIe_Interposer_Cable_Connector	CPU 1: Ports 1A through 1B (x8 electrical, x8 mechanical)	N/A

The PCIe interposer riser card option is designed to install into the Interposer Riser slot on the server board and supports the following features:

- One LP/HL, single-width PCIe add-in card slot (x8 electrical, x8 mechanical)
- One x8 PCIe MCIO connector
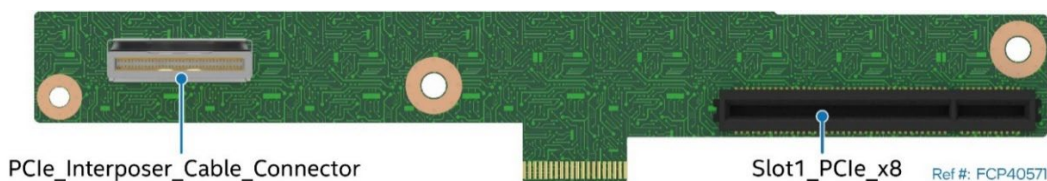
Figure 53. PCIe* Interposer Riser Card

Table 44. PCIe* Interposer Riser Card Connector Description

Connector	Description	Maximum Available Power (W)
Slot1_PCIe_x8	CPU 1: Ports 1A through 1B (x8 electrical, x8 mechanical)	25
PCIe_Interposer_Cable_Connector	CPU 1: Ports 1A through 1B (x8 electrical, x8 mechanical)	N/A

To use the interposer riser card, the PCIe interposer cable must be installed to the matching x8 PCIe MCIO* connectors found on the PCIe MCIO riser card and the PCIe Interposer card as shown below.
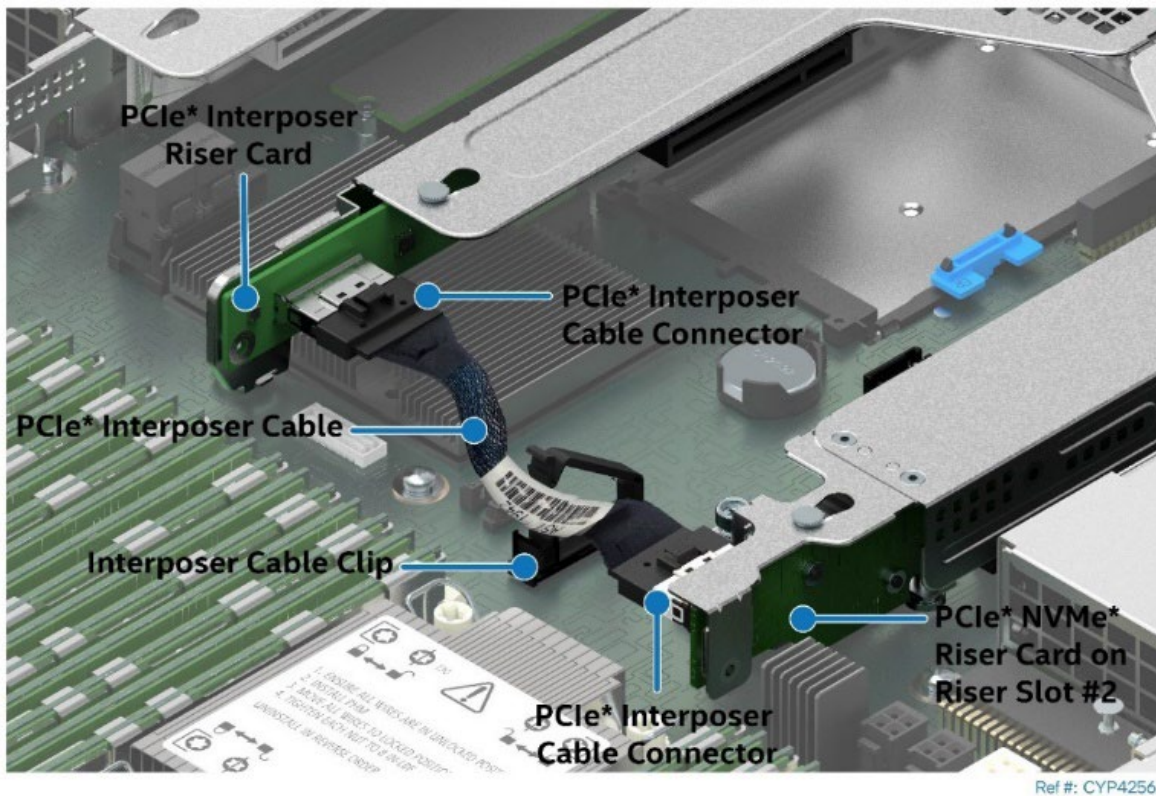
Figure 54. PCIe* Interposer Riser Card to PCIe* Riser Card Connectivity

Table 45. PCIe* Interposer Riser Slot Pinout

Pin #	PCIe* Signal (from processor perspective)	Pin #	PCIe* Signal (from processor perspective)
A1	GND	B1	GND
A2	Spare	B2	Spare
A3	Spare	B3	Spare
A4	GND	B4	GND
A5	12V	B5	12V
A6	12V	B6	12V
A7	GND	B7	GND
A8	12V	B8	12V
A9	12V	B9	12V
A10	GND	B10	GND
A11	3.3VAUX	B11	Spare
A12	3.3V PWRGD	B12	Spare
A13	GND	B13	GND
A14	SMBus Clock	B14	Spare
A15	SMBus Data	B15	Spare
A16	GND	B16	GND
A17	FRU/Temp ADDR [l]	B17	PERST_N
A18	PWRBRK_N	B18	PE_WAKE_N
A19	GND	B19	GND
A20	REFCLK_TOP_P	B20	Riser ID[0]
A21	REFCLK_TOP_N	B21	Riser ID[1]
A22	GND	B22	GND

Pin #	PCIe* Signal (from processor perspective)
A23	Spare
A24	Spare
A25	GND
A26	Spare
A27	Spare
A28	GND

Pin #	PCIe* Signal (from processor perspective)
B23	SYS_THROTTLE_N
B24	MUX_RST_N
B25	GND
B26	Spare
B27	Spare
B28	GND

Pin #	PCIe* Signal (from processor perspective)

Pin #	PCIe* Signal (from processor perspective)

9.   Onboard Storage Support Options

The Intel® Server Board M50FCP2SBSTD includes various onboard connectors to support different SATA 3.0 and NVMe storage options.

- Two M.2 PCIe*/SATA SSD connectors
- Two 4-port SATA 3.0 SFF-8643 Mini-SAS HD cable connectors
- Sixteen PCIe MCIO* cable connectors for NVMe* support

Support for different storage options varies depending on the system configuration and/or available accessory options installed. This chapter provides an overview for each onboard storage support option.

9.1   Server Board SATA Support

SATA drives are supported by two Intel chipset embedded AHCI SATA controllers, identified as "SATA_0" and "SATA_1". Each SATA controller supports 6 GB/s SATA 3.0 ports. SATA ports from each controller are routed to connectors on the server board as follows:

- SATA_0 ports 0-3 are routed to one SFF-8643 MiniSAS HD cable connector
- SATA_1 ports 0–3 are routed to one SDD-8643 Mini-SAS HD cable connector
- SATA_1 ports 4 and 6 are routed to two M.2 SSD connectors (See Section 9.2)
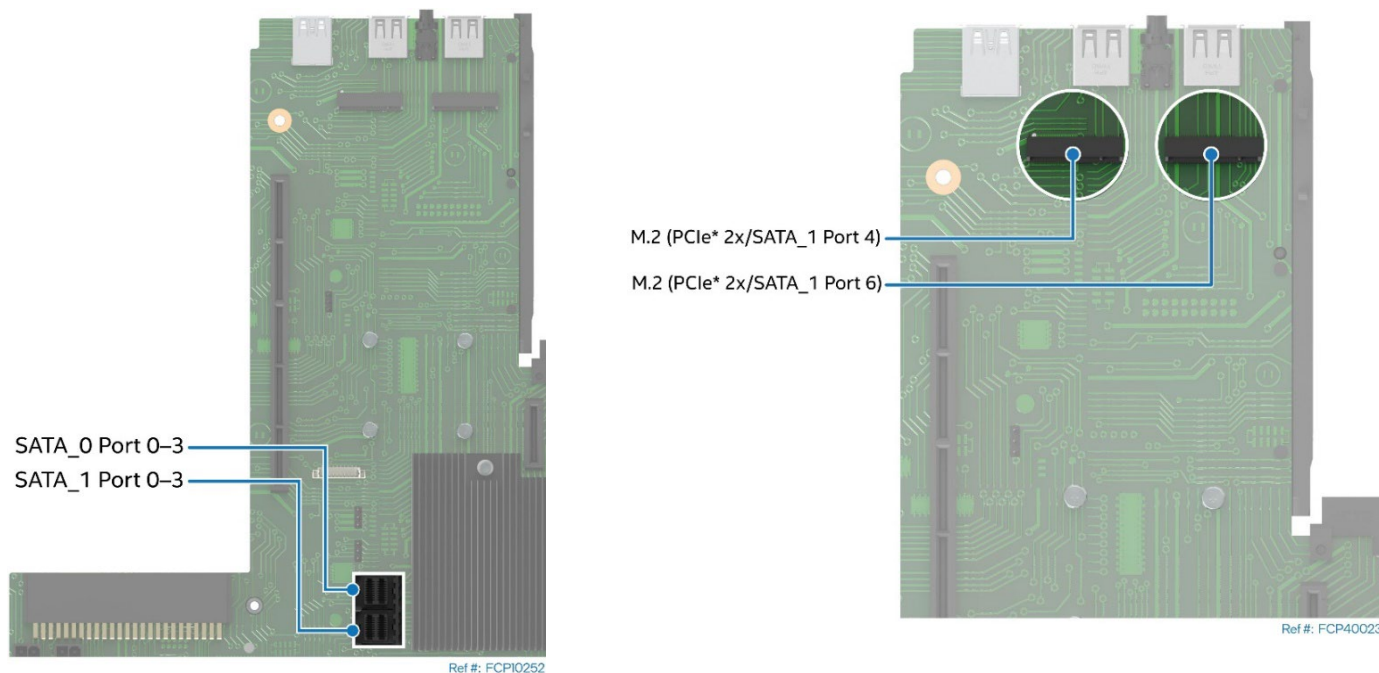
Figure 55. Onboard SATA Cable Connectors and M.2 SSD Connectors

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The following table describes the SATA_0 and SATA_1 controller feature support.

Table 46. SATA_0 and SATA_1 Controller Feature Support

Feature	Description	AHCI Mode
Native Command Queuing (NCQ)	Allows the device to reorder commands for more efficient data transfers	Supported
Auto Activate for direct memory access (DMA)	Collapses a DMA Setup, then DMA Activate sequence into a DMA Setup only	Supported
Hot Plug Support (U.2 Drives Only)	Allows for device detection without power being applied and ability to connect and disconnect devices without prior notification to the system	Supported
Asynchronous Signal Recovery	Provides a recovery from a loss of signal or establishing communication after hot plug	Supported
6 Gb/s Transfer Rate	Capable of data transfers up to 6 Gb/s	Supported
ATAPI Asynchronous Notification	A mechanism for a device to send a notification to the host that the device requires attention	Supported
Host and Link Initiated Power Management	Capability for the host controller or device to request Partial and Slumber interface power states	Supported
Staggered Spin-Up	Enables the host the ability to spin up hard drives sequentially to prevent power load problems on boot	Supported
Command Completion Coalescing	Reduces interrupt and completion overhead by allowing a specified number of commands to complete and then generating an interrupt to process the commands	Supported

The SATA_0 controller and the SATA_1 controller can be independently configured using the <F2> BIOS setup utility to function in AHCI mode or disabled.

9.1.1   Staggered Disk Spin-Up

A high number of hard drives with spinning media can be attached to the onboard SATA controllers. The combined startup power demand for all attached hard drives can be much higher than the normal running power requirements.

To mitigate the condition and lessen the peak power demand during system startup, both the AHCI SATA controllers implement a Staggered Spin-Up capability for the attached drives. This means that the drives are started up separately, with a certain delay between disk drives starting.

To enable staggered spin-up, go to BIOS setup utility >Mass Storage Controller Configuration screen > **AHCI HDD Staggered Spin-Up**.

9.2   M.2 SSD Storage Support

The server board includes two M.2 SSD connectors (See Figure 55). The connectors are labeled "*M2_x2PCIE/SATA_1 Port 4*" and "*M2_x2PCIE/SATA_1 Port 6*". Each M.2 slot can support either a PCIe NVMe SSD or SATA SSD that conforms to a 22110 (110 mm) or 2280 (80 mm) form factor.

Each M.2 slot is connected to two PCIe 3.0 lanes from the chipset's embedded controller.

9.3   NVMe* Storage Support

Non-Volatile Memory Express (NVMe) is an optimized, high-performance scalable storage interface designed to address the needs of enterprise systems that use PCIe-based solid-state storage. NVMe provides efficient access to non-volatile memory storage devices. The NVMe technology allows Intel server boards to take advantage of the levels of parallelism possible in modern SSDs.

9.3.1   PCIe* Mini Cool Edge IO (MCIO*) Connector Support

The server board includes sixteen PCIe Mini Cool Edge IO (MCIO*) cable connectors. MCIO is a next generation ultra-high-speed interconnect solution for server boards and storage devices. Each MCIO cable connector supplies X4 PCIe bus lanes for a PCIe NVMe drive when cabled to a backplane.

X32 PCIe bus lanes from each installed processor are routed to a set of eight PCIe MCIO connectors (See Figure 14). On the server board each MCIO connector is label according to the processor supplying the PCIe bus lanes, and the PCIe port from the specified processor (See Figure 56).
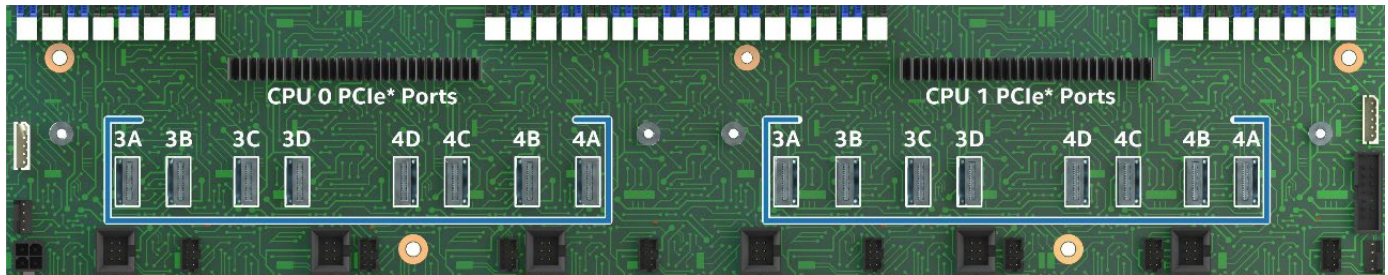
Ref #: FCP10091

Figure 56. PCIe* MCIO Connectors

9.3.2   Volume Management Device (VMD) for NVMe* for Linux*

Volume Management Device (VMD) is hardware logic inside the processor root complex to help manage PCIe NVMe SSDs. VMD provides robust hot plug support and status LED management using embedded Linux* VMD drivers. This allows servicing of storage system NVMe SSD media without concern of system crashes or hangs when ejecting or inserting NVMe SSD devices on the PCIe bus.
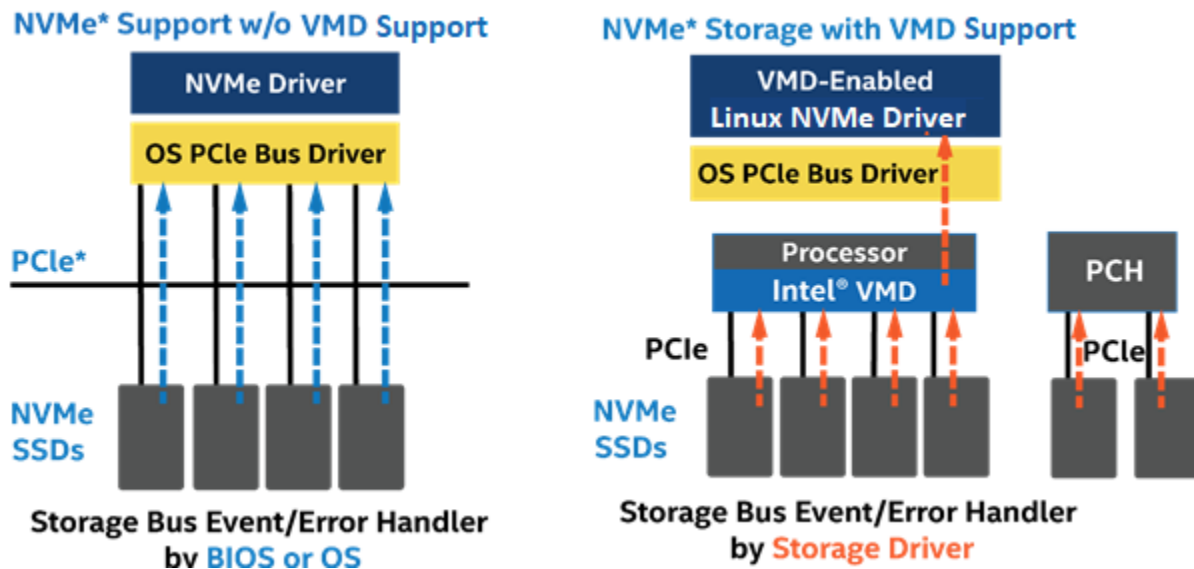
Figure 57. NVMe* Storage Bus Event / Error Handling

VMD includes the following features and capabilities:

- Hardware is integrated inside the processor PCIe root complex.
- Entire PCIe trees are mapped into their own address spaces (domains).
- Each domain manages x16 PCIe lanes.
- Can be enabled/disabled through the <F2> BIOS setup utility at x4 lane granularity.

- OS Embedded driver sets up/manages the domain (enumerate, event/error handling).
- Hot plug support - hot insert array of PCIe NVMe SSDs.
- Support for PCIe NVMe SSDs only. No network interface controllers (NICs), graphics cards, etc.
- Maximum of 128 PCIe bus numbers per domain.
- Support for Management Component Transport Protocol (MCTP) over SMBus only.
- Support for MMIO only (no port mapped I/O).
- Does not support NTB, Intel® QuickData Technology, Intel® Omni-Path Architecture (Intel® OPA), or SR-IOV.
- Correctable errors do not bring down the system.
- VMD only manages devices on PCIe lanes routed directly from the processor or chipset PCH.
- When VMD is enabled, the BIOS does not enumerate devices that are behind VMD. The OS embedded VMD-enabled driver is responsible for enumerating these devices and exposing them to the host.

9.3.2.1   Enabling VMD for NVMe* Support

For installed NVMe devices to use the VMD features in the system, VMD must be enabled on the appropriate processor PCIe root ports in the <F2> BIOS setup utility. By default, VMD support is disabled on all processor PCIe* root ports. To enable VMD support on the appropriate CPU PCIe root port, navigate to **Advanced > PCI Configuration > Volume Management Device** in the <F2> BIOS Setup menu.

Note: PCIe root ports should only be enabled for PCIe MCIO connectors supporting NVMe devices. PCIe root ports supporting other Non-NVMe PCIe devices should remain in their default disabled setting.

The following table provides the PCIe port routing information for the server board PCIe MCIO connectors.

Table 47. CPU to PCIe* NVMe* MCIO Connector Routing

Host	CPU Port	Routed to MCIO Connector
CPU 0	Port 3A	CPU0_PCIe_Port3A
	Port 3B	CPU0_PCIe_Port3B
	Port 3C	CPU0_PCIe_Port3C
	Port 3D	CPU0_PCIe_Port3D
	Port 4D	CPU0_PCIe_Port4D
	Port 4C	CPU0_PCIe_Port4C
	Port 4B	CPU0_PCIe_Port4B
	Port 4A	CPU0_PCIe_Port4A
CPU 1	Port 3A	CPU1_PCIe_Port3A
	Port 3B	CPU1_PCIe_Port3B
	Port 3C	CPU1_PCIe_Port3C
	Port 3D	CPU1_PCIe_Port3D
	Port 4D	CPU1_PCIe_Port4D
	Port 4C	CPU1_PCIe_Port4C
	Port 4B	CPU1_PCIe_Port4B
	Port 4A	CPU1_PCIe_Port4A

10. System I/O

This chapter provides information on the server board serial ports, USB ports, and Video support.

10.1 Serial Port A Support

Serial Port A is an external RJ45 type connector on the back edge of the server board.
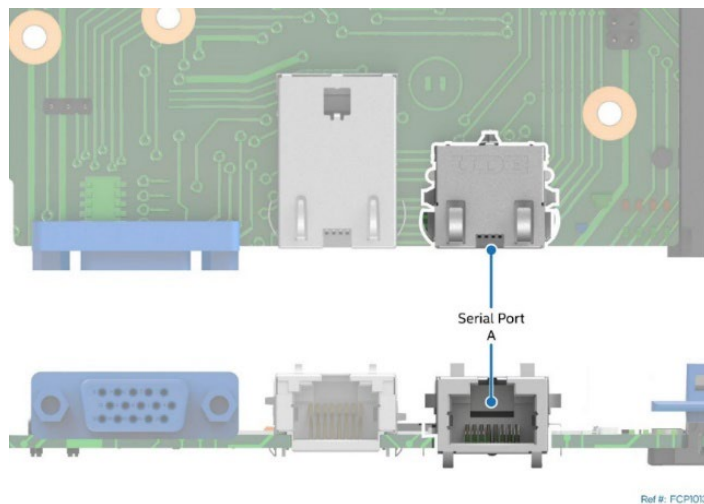
Figure 58. Serial Port A

The pin orientation is shown in Figure 59 and the pinout is in Table 48.
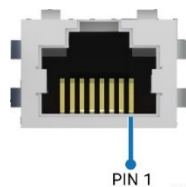
Figure 59. RJ45 Serial Port A Pin Orientation

Table 48. RJ45 Serial Port A Connector Pinout

Pin #	Signal Name
1	RTS
2	DTR
3	SOUT
4	GROUND
5	RI
6	SIN
7	DCD or DSR
8	CTS

10.2 USB Support

The following figure shows the three rear USB ports located on the back edge of the server board. The USB 3.0 port is farthest from the OCP module connector.
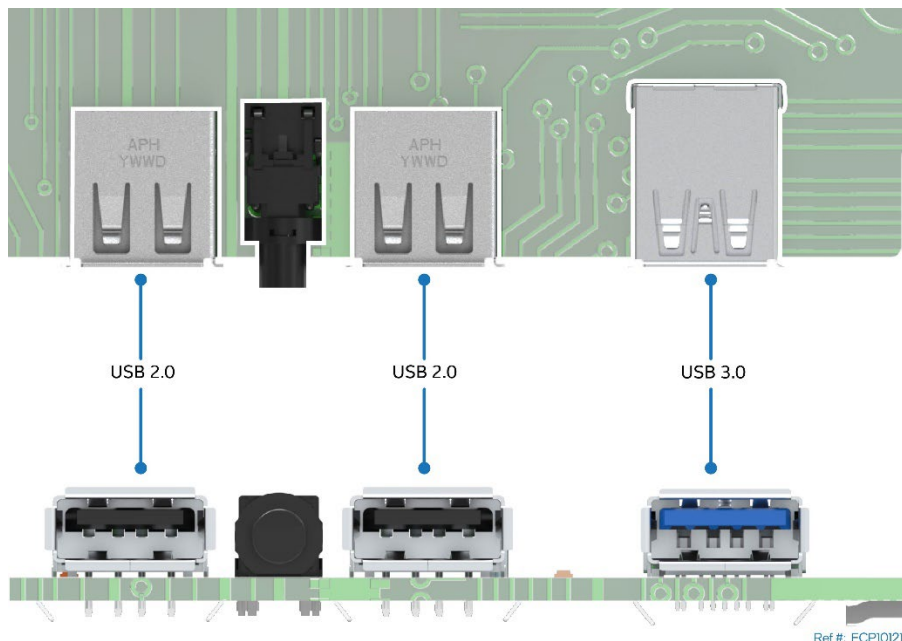
Figure 60. External USB 2.0 and 3.0 Connector Ports

The following table provides the pinout for each connector.

Table 49. USB 3.0 Rear Connector Pinout

Pin #	Signal Name
1	VBUS
2	D-1
3	D+1
4	GND
5	SSRX-1
6	SSRX+1
7	GND_DRAIN
8	SSTX-1
9	SSTX+1
GND1	GND
GND2	GND

Table 50. USB 2.0 Rear Connector Pinouts

Pin #	Signal Name
1	PWR
2	D-
3	D+
4	GND
GND1	GND
GND2	GND

10.3 Video Support

The server board has two video connectors:

- A standard DE-15 VGA connector is on the back edge of the server board.
- A 7X2 (14-pin) VGA header (J21) is on the front right corner of the server board. This header can be used to provide an alternate front panel VGA video connector. Concurrent use of both the front panel and back panel VGA connectors is not supported. Logic designed into the VGA support circuitry will disable the VGA connector on the back panel when it detects that a monitor is attached to the front panel video connector.

Table 51. VGA Header (J21) pinout

Signal Name	Pin#	Pin#	Signal Name
MOD_VOS_FRONT_RED	1	2	GND
MOD_VOS_FRONT_GREEN	3	4	GND
MOD_VOS_FRONT_BLUE	5	6	GND
VS_MID	7	8	GND
HS_MID	9	10	key
I2C_VIDMID_SDA	11	12	FM_V_FRONT_PRES_N
I2C_VIDMID_SCL	13	14	TP_VID_FNT_CONN

10.3.1   Video Resolutions

The graphics controller of the Aspeed AST2600* SMP is VGA-compliant controller with 2D hardware acceleration and full bus primary support. With 16 MB of memory reserved, the video controller supports the resolutions in the following table.

Table 52. Supported Video Resolutions

2D Mode Resolution	2D Video Support (Color Bit)			
	8 bpp	16 bpp	24 bpp	32 bpp
640 x 480	60, 72, 75, 85	60, 72, 75, 85	Not supported	60, 72, 75, 85
800 x 600	60, 72, 75, 85	60, 72, 75, 85	Not supported	60, 72, 75, 85
1024 x 768	60, 72, 75, 85	60, 72, 75, 85	Not supported	60, 72, 75, 85
1152 x 864	75	75	75	75
1280 x 800	60	60	60	60
1280 x 1024	60	60	60	60
1440 x 900	60	60	60	60
1600 x 1200	60	60	Not supported	Not supported
1680 x 1050	60	60	Not supported	Not supported
1920 x 1080	60	60	Not supported	Not supported
1920 x 1200	60	60	Not supported	Not supported

10.3.2   Server Board Video and Add-In Video Adapter Support

The BIOS setup utility includes options to support the desired video operation when an add-in video card is installed.

- When both the **Onboard Video** and **Add-In Video Adapter** options are set to **Enabled**, both video displays can be active. The onboard video is still the primary console and active during BIOS POST. The add-in video adapter is only active under an operating system environment with video driver support.

- When **Onboard Video** is **Enabled** and **Add-In Video Adapter** is **Disabled**, only the onboard video is active.
- When **Onboard Video** is **Disabled** and **Add-In Video Adapter** is **Enabled**, only the add-in video adapter is active.

Configurations with add-in video cards can get more complicated with a dual processor board. Some multi-socket boards have PCIe slots capable of hosting an add-in video card that is attached to the IIOs of processor sockets other than processor Socket 0. However, only one processor socket can be designated as a legacy VGA socket as required in POST. To provide for this situation, there is the PCI Configuration option **Legacy VGA Socket**. The rules for this option are:

- The **Legacy VGA Socket** option is grayed out and unavailable unless an add-in video card is installed in a PCIe slot supported by CPU 1.
- Because the onboard video is hardwired to CPU 0, when **Legacy VGA Socket** is set to **CPU Socket 1**, the onboard video is disabled.

10.3.3   Dual Monitor Support

The BIOS supports single and dual video when add-in video adapters are installed. The BIOS setup utility does not have an enable/disable option for dual video. It works when both the **Onboard Video** and **Add-In Video Adapter** options are enabled.

In the single video mode, the onboard video controller or the add-in video adapter is detected during POST.

In dual video mode, the onboard video controller is enabled and is the primary video device. The add-in video adapter is allocated resources and is considered as the secondary video device during POST. The add-in video adapter is not active until the operating system environment is loaded.

10.4 Intel® Ethernet Network Adapter for OCP* Support

The server board supports several types of Intel® Ethernet Network Adapters. Supported adapters adhere to the Open Compute Project (OCP) 3.0 specification, which utilize an edge connector interface to the server board, allowing it to be serviced from the back of the chassis instead of having to access the inside of the chassis to install or remove it.

Note: Reference the *Intel® Server M50FCP Family Configuration Guide* for a list of supported adapter cards.
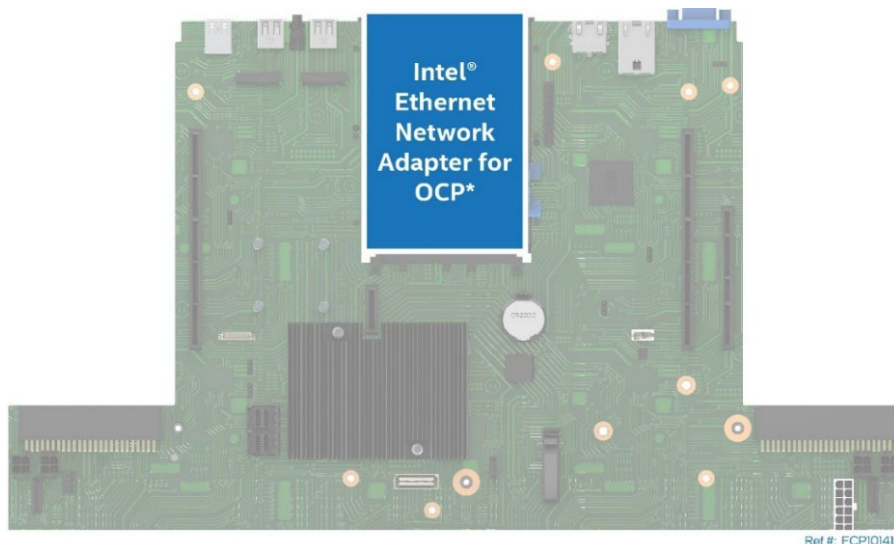
Figure 61. Intel® Ethernet Network Adapter for OCP* Placement

The following figures illustrate possible installation of an OCP 3.0 add-in card into a server chassis. Chassis design and fastener type of the chosen card (Internal lock or Pull tab with fastener screw) will determine how the card is securely kept in place.

Figure 62. OCP 3.0 Add-in Card Installation – Pull Tab with Fastener Screw Option

Ref #: FCP40141
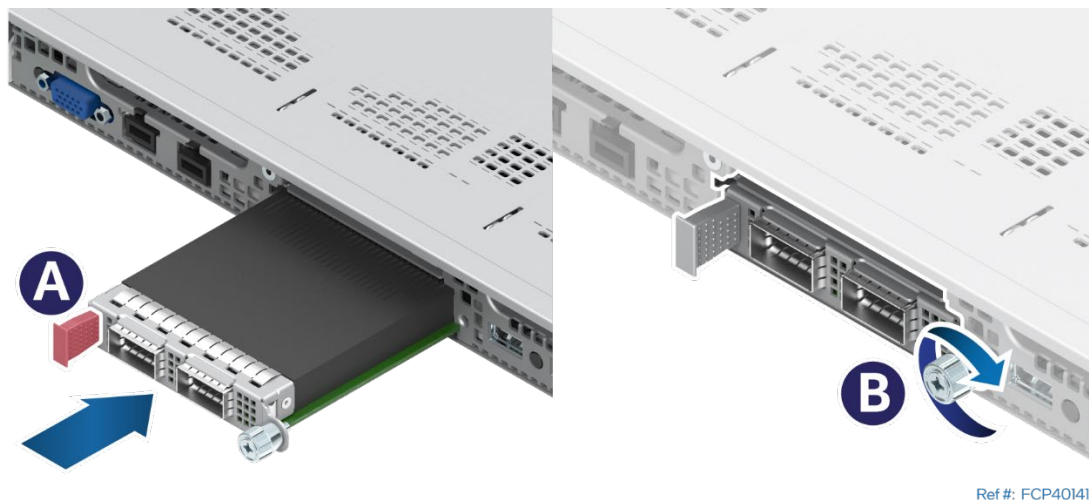
Figure 63. OCP 3.0 Add-in Card Installation – Internal Lock Option

CYP41200

11. Intel Light-Guided Diagnostics

This chapter provides an overview of the diagnostic LEDs found on the server board. LEDs include: Post Code Diagnostic LEDs, System ID LED, CPU 0 and CPU 1 Fault LEDs, and Fan Fault LEDs (for 8-pin fan connectors only). The following figure shows the location of the LEDs on the server board.
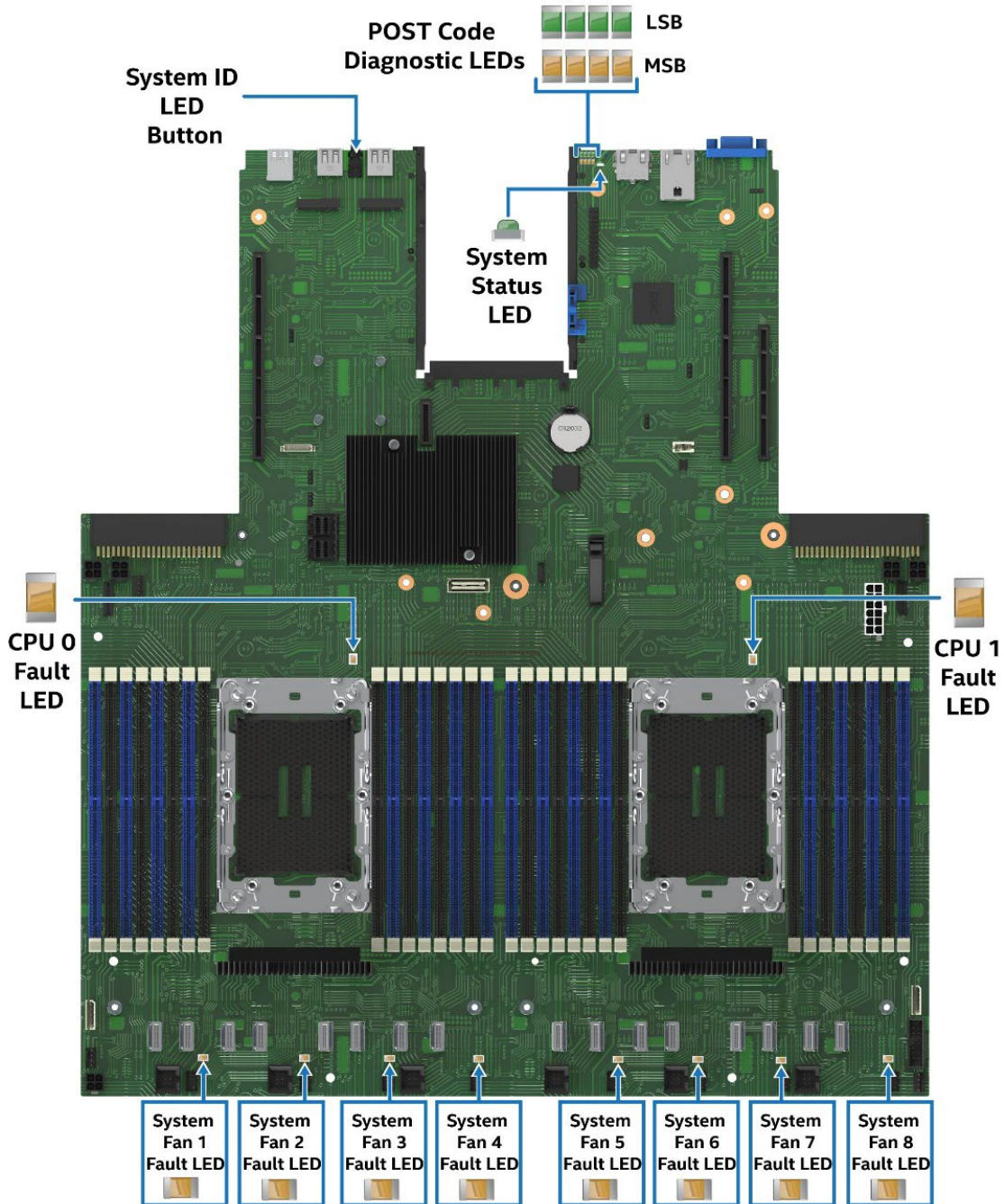
Figure 64. Intel® Light-Guided Diagnostics: LED Identification

Note: The System Fan Fault LEDS in the Figure 64 are only for the 8-pin fan connectors.

The following figure provides an exploded view of the POST code Diagnostic, System ID, and System Status LEDs area.
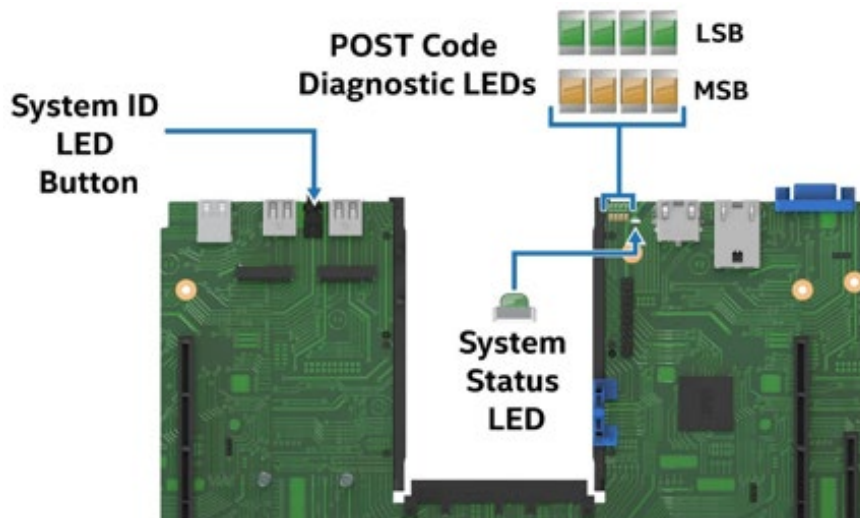
Figure 65. POST Code Diagnostic, System ID, and System Status LED Area

11.1 Post Code Diagnostic LEDs

As an aid in troubleshooting a system hang that occurs during a system POST process, the server board includes a bank of eight (2X4) diagnostic LEDs on the back edge of the server board. These diagnostic LEDs are used to represent hexadecimal POST progress codes or halt error codes for memory initialization and platform configuration routines from the memory reference code (MRC) and system BIOS.

If a system hangs during POST execution, the displayed POST progress code can be used to identify the last POST routine that was run before the error occurred, helping to isolate the possible cause of the hang condition even when video is not available. See Appendix C for a complete description of how these LEDs are read, and for a list of all supported POST codes.

11.2 System ID LED

The server board includes a System ID Button with an integrated blue LED on the back edge of the server board. This LED is used to visually identify a specific server system from the back of the system when installed in a rack among many other similar systems.
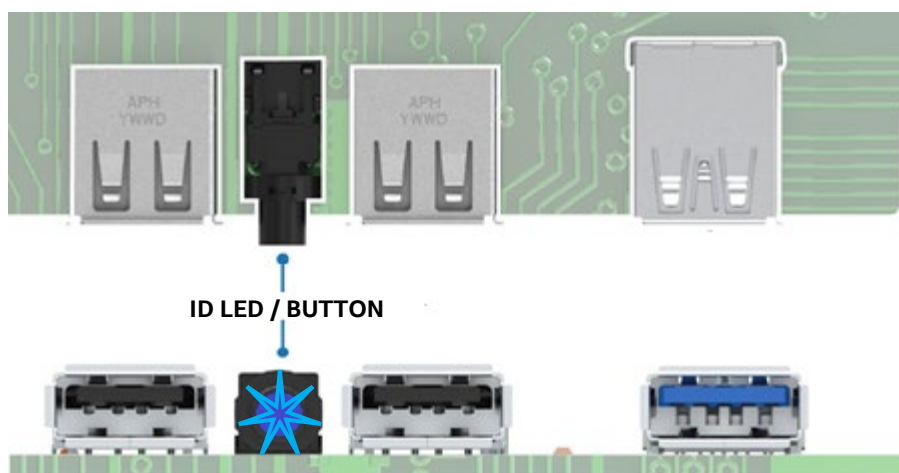
Figure 66. System ID LED / Button

The LED state can be changed using any of three methods:

- Press the System ID LED button located on the back edge of the server board. This option produces a solid on state and will cause the LED to stay illuminated until the button is pressed, turning it off.
- Press the System ID LED on the system front panel (If configured). This option produces a solid on state and will cause the LED to stay illuminated until the button is pressed, turning it off.
- Issue an IPMI Chassis Identify command. This option causes the System ID LED to blink for up to 2 minutes.

11.3 System Status LED

The server board includes a bi-color system status LED. This LED indicates the current health of the server. Possible LED states include solid green, blinking green, solid amber, and blinking amber.

When the server is powered down (transitions to the DC-off state or S5), the BMC is still on standby power and retains the sensor and front panel status LED state established before the power-down event.

When source power is first applied to the system, the status LED turns solid amber, and then immediately changes to blinking green to indicate that the BMC is booting. If the BMC boot process completes with no errors, the status LED changes to solid green.

The following table lists and describes the states of the system status LED.

Table 53. System Status LED State Definitions

LED State	System State	BIOS Status Description
Off	No AC Power to system	- System power is not present. - System is in EuP Lot 6 off mode.
Solid green	System is operating normally.	- System is in S5 soft-off state. - System is running (in S0 State) and its status is healthy. The system is not exhibiting any errors. Source power is present, BMC has booted, and manageability functionality is up and running. - After a BMC reset, and with the chassis ID solid on, the BMC is booting Linux*. Control has been passed from BMC U-Boot* to BMC Linux*. The BMC is in this state for roughly 10–20 seconds.
Blinking green	System is operating in a degraded state although still functioning, or system is operating in a redundant state but with an impending failure warning.	- Redundancy loss such as power-supply or fan. Applies only if the associated platform subsystem has redundancy capabilities. - Fan warning or failure when the number of fully operational fans is still more than the minimum number needed to cool the system. - Non-critical threshold crossed: temperature (including HSBP temp and processor Thermal Control (Therm Ctrl) sensors), voltage, input power to power supply, output current to main power rail. - Power supply predictive failure occurred while redundant power supply configuration was present. - Unable to use all installed memory (more than 1 memory module installed). - Correctable Errors over a threshold and migrating to a spare memory module (memory sparing). This indicates that the system no longer has spared DIMMs (a redundancy lost condition). Corresponding memory module LED lit. - In mirrored configuration, when memory mirroring takes place and system loses memory redundancy. - Battery failure. - BMC executing in U-Boot. (Indicated by Chassis ID LED blinking at 3 Hz while Status LED blinking at 1 Hz). System in degraded state (no manageability). BMC U-Boot is running but has not transferred

LED State	System State	BIOS Status Description
Blinking Green (Cont.)		control to BMC Linux*. Server is in this state 6–8 seconds after BMC reset while it pulls the Linux* image from flash. • BMC Watchdog has reset the BMC. • Power Unit sensor offset for configuration error is asserted. • SSD Hot Swap Controller is off-line or degraded.
Blinking green and **amber**	System is initializing after source power is applied	• PFR in the process of updating/authenticating/recovering when source power is connected. system firmware being updated. • System not ready to take power button event/signal.
Blinking amber	System is operating in a degraded state with an impending failure warning, although still functioning. System is likely to fail.	• Critical threshold crossed: Voltage, temperature (including HSBP temp), input power to power supply, output current for main power rail from power supply and PROCHOT (Therm Ctrl) sensors. • VRD Hot asserted. • Minimum number of fans to cool the system not present or failed. • Hard drive fault. • Power Unit Redundancy sensor: Insufficient resources offset (indicates not enough power supplies present). • In non-sparing and non-mirroring mode, if the threshold of correctable errors is crossed within the window. • Invalid firmware image detected during boot or firmware update
Solid amber	Critical/non-recoverable: system is halted. Fatal alarm: system has failed or shut down.	• Processor CATERR signal asserted. • MSID mismatch detected (CATERR also asserts for this case). • CPU 0 is missing. • Processor Thermal Trip. • No power good: power fault. • Memory module failure when there is only 1 memory module present and hence no good memory present. • Runtime memory uncorrectable error in non-redundant mode. • Memory module Thermal Trip or equivalent. • SSB Thermal Trip or equivalent. • Processor ERR2 signal asserted. • BMC/Video memory test failed. (Chassis ID shows blue/solid-on for this condition.) • Both U-Boot BMC firmware images are bad. (Chassis ID shows blue/solid-on for this condition.) • 240 VA fault. • Fatal Error in processor initialization: o Processor family not identical o Processor model not identical o Processor core/thread counts not identical o Processor cache size not identical o Unable to synchronize processor frequency o Unable to synchronize QPI link frequency • BMC fail authentication with non-recoverable condition, system hang at T-1; boot PCH only, system hang; PIT failed, system lockdown.

11.4 BMC Boot / Reset Status LED Indicators

During the BMC boot or BMC reset process, the system status LED and System ID LED are used to indicate BMC boot process transitions and states (if present). A BMC boot occurs when the AC power is first applied (DC power on/off does not reset BMC). BMC reset occurs after a BMC firmware update, on receiving a BMC cold reset command, and following a reset initiated by the BMC watchdog. The following table defines the LED states during the BMC boot/reset process.

Table 54. BMC Boot / Reset Status LED Indicators

BMC Boot/Reset State	System ID LED	System Status LED	Comment
BMC/video memory test failed	Solid blue	Solid amber	Non-recoverable condition. Contact an Intel® representative for information on replacing this motherboard.
Both universal bootloader (U-Boot) images bad	6 Hz blinking blue	Solid amber	Non-recoverable condition. Contact an Intel® representative for information on replacing this motherboard.
BMC in U-Boot	3 Hz blinking blue	1 Hz blinking green	Blinking green indicates degraded state (no manageability), blinking blue indicates that U-Boot is running but has not transferred control to BMC Linux*. Server is in this state 6–8 seconds after BMC reset while it pulls the Linux* image into flash.
BMC booting Linux*	Solid blue	Solid green	After an AC cycle/BMC reset, indicates that the control has been passed from U-Boot to BMC Linux itself. The BMC is in this state for 10-20 seconds.
End of BMC boot/reset process. Normal system operation	Off	Solid green	Indicates that BMC Linux has booted and manageability functionality is up and running. Fault/status LEDs operate as usual.

11.5 Processor Fault LEDs

The server board includes a processor fault LED for each processor socket. The processor fault LED is lit if an MSID mismatch error is detected (that is, processor power rating is incompatible with the board).

Table 55. Processor Fault LED State Definition

Component	Managed by	Color	State	Description
Processor Fault LEDs	BMC	Off	Off	Ok (no errors)
		Solid Amber	On	MSID mismatch
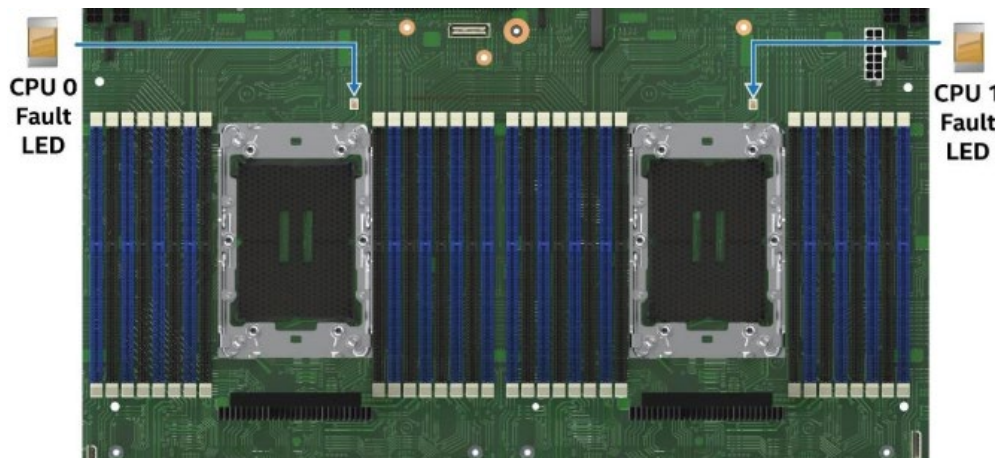
Figure 67. Processor Fault LEDs

11.6 Memory Fault LEDs

The server board includes memory fault LEDs for each memory module slot (see following figure). When the BIOS detects a memory fault condition, it sends an IPMI OEM command (`Set Fault Indication`) to the BMC to turn on the associated memory slot fault LED. These LEDs are only active when the system is in the on state. The BMC does not activate or change the state of the LEDs unless instructed by the BIOS.

Table 56. Memory Fault LED State Definition

Component	Managed by	Color	State	Description
Memory Fault LED	BMC	Off	Off	Memory working correctly
		Solid amber	On	Memory failure: detected by the BIOS
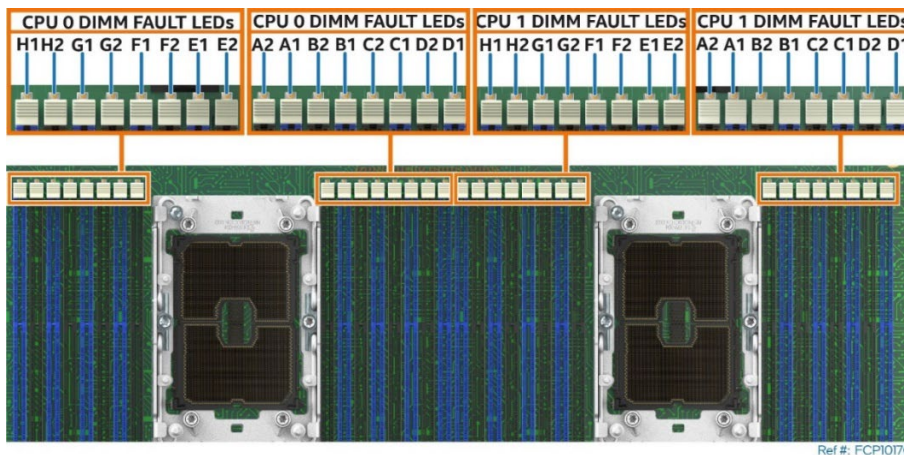
Figure 68. Memory Fault LED Location

11.7 Fan Fault LEDs

The following figure shows the location of the fan fault LEDs associated with the 8-pin system fan connectors. The BMC lights a fan fault LED if it detects that the fan-tach sensor of the associated fan connector has a lower critical threshold event status asserted. Fan-tach sensors are manual re-arm sensors. Once the lower critical threshold is crossed, the LED remains lit until the sensor is re-armed. These sensors are re-armed at system DC power-on and system reset.

Table 57. Fan Fault LED State Definition

Component	Managed by	Color	State	Description
Fan Fault LED	BMC	Off	Off	Fan working correctly
		Solid Amber	On	Fan failed
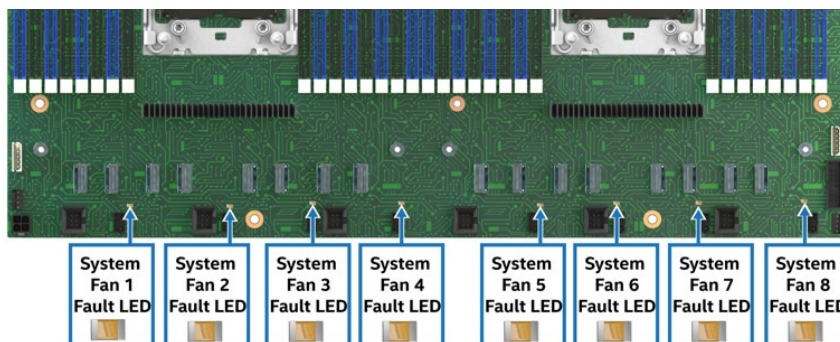
Figure 69. 8–Pin Fan Fault LEDs

12. System Security

The server board supports a variety of system security options designed to prevent unauthorized system access or tampering with server settings. System security options supported include:

- Password protection
- Front panel lockout
- Intel® Platform Firmware Resilience (Intel® PFR) Technology
- Intel® Software Platform Guard Extensions (Intel® SGXPFR) Technology
- Intel® Total Memory Encryption – Multi-Key (Intel® TME-MK) Technology
- Trusted platform module (TPM) support
- Converged Intel® Boot Guard and Trusted Execution Technology (Intel® TXT)
- Unified Extensible Firmware Interface (UEFI) Secure Boot Technology

12.1 Password Protection

The <F2> BIOS setup utility includes a Security tab where options to configure passwords, front panel lockout, and TPM settings, can be found.
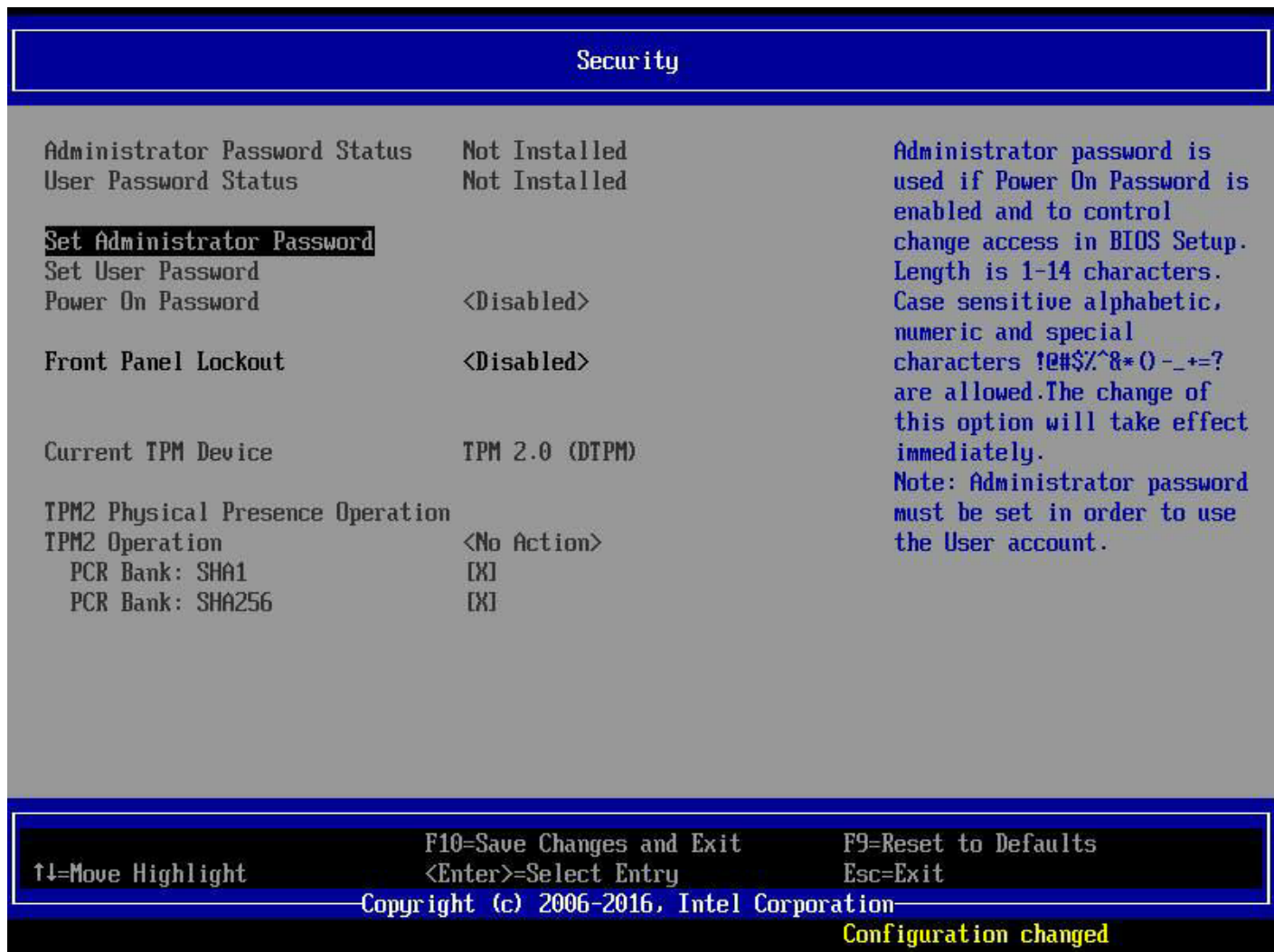
Figure 70. BIOS Setup Utility Security Tab

12.1.1 Password Setup

The BIOS uses passwords to prevent unauthorized access to the server board. Passwords can restrict entry to the BIOS setup utility, restrict use of the Boot Device popup menu during POST, suppress automatic USB device re-ordering, and prevent unauthorized system power-on. Intel® strongly recommends that an administrator password be set. A system with no administrator password set allows anyone who has access to the server to change BIOS settings.

- An administrator password must be configured to set the user password.
- The maximum length of a password is 14 characters.
- The minimum length is one character.
- The password can be made up of a combination of alphanumeric (a-z, A-Z, 0–9) characters and any of the following special characters: ! @ # $ % ^ & * ( ) - _ + = ?
- Passwords are case sensitive.
- The administrator and user passwords must be different from each other.
- An error message is displayed, and a different password must be entered if there is an attempt to enter the same password for both.

The use of strong passwords is encouraged, but not required. To meet the criteria for a strong password, the password entered must be at least eight characters in length. It must include at least one each of alphabetical, numeric, and special characters. If a weak password is entered, a warning message is displayed, and the weak password is accepted. Once set, a password can be cleared by changing it to a null string. This action requires the administrator password and must be done through the BIOS setup utility. Clearing the administrator password also clears the user password. Passwords can also be cleared by using the password clear jumper on the server board. For more information on the password clear jumper, see Section 13.2.

Resetting the BIOS configuration settings to default values (by any method) has no effect on the administrator and user passwords.

As a security measure, if a user or administrator enters an incorrect password three times in a row during the boot sequence, the system is placed into a halt state. A system reset is required to exit out of the halt state. This feature makes it more difficult to guess or break a password.

In addition, on the next successful reboot, the Error Manager displays a Major Error code 0048. A SEL event is also logged to alert the authorized user or administrator that a password access failure has occurred.

12.1.2 System Administrator Password Rights

When the correct administrator password is entered, the user may perform the following actions:

- Access the BIOS setup utility.
- Configure all BIOS setup options in the BIOS setup utility.
- Clear both the administrator and user passwords.
- Access the Boot Menu during POST.

If the Power-on Password function is enabled in the BIOS setup utility, the BIOS halts early in POST to request a password (administrator or user) before continuing POST.

12.1.3 Authorized System User Password Rights and Restrictions

When the correct user password is entered, the user can perform the following actions:

- Access the BIOS setup utility.
- View, but not change, any BIOS setup options in the BIOS setup utility.
- Modify system time and date in the BIOS setup utility.

If the Power-on Password function is enabled in the BIOS setup utility, the BIOS halts early in POST to request a password (administrator or user) before continuing POST.

Configuring an administrator password imposes restrictions on booting the system and configures most setup fields to read-only if the administrator password is not provided. The boot popup menu requires the administrator password to function, and the USB reordering is suppressed if the administrator password is enabled. Users are restricted from booting in anything other than the boot order defined in setup by an administrator.

12.2 Front Panel Lockout

If enabled in the BIOS setup utility from the Security screen, this option disables the following front panel features:

- The off function of the power button.
- System reset button.

If front panel lockout is enabled, system power off and reset must be controlled via a system management interface.

12.3 Intel® Platform Firmware Resilience (Intel® PFR) 3.0

As the intensity, sophistication, and disruptive impact of security attacks continue to escalate, data centers are driving a holistic approach to protect their critical infrastructure. This approach includes protecting server systems at the firmware level, the lowest layers of the platform, where threats are most difficult to detect. To address this situation, Intel has developed Intel® PFR technology where platforms can provide security starting with power-on, system boot, and OS load activities.

The Intel® Server Board M50FCP2SBSTD supports Intel® PFR technology, a hardware-enhanced platform security that uses an Intel® FPGA to protect, detect, and recover platform firmware.

- **Protect:** Monitors and filters malicious traffic on system buses. All platform firmware is attested safe before code execution.
- **Detect:** Verifies integrity of platform firmware images before executing. Performs boot and runtime monitoring to assure server is running a known good firmware.
- **Recover:** Automatically restores corrupted firmware from a protected gold recovery image within minutes.

Critical firmware elements protected in an Intel® Server Board M50FCP2SBSTD include: BIOS, SPI descriptor, BMC, Intel® Management Engine (Intel® ME), and power supply firmware. This capability to mitigate firmware corruption is an important industry innovation and provides an optimal solution for security-sensitive organizations.

Intel® PFR fully supports the National Institute of Standards and Technology (NIST*) proposed firmware resiliency guidelines (SP 800–193) that have wide industry support.

12.4 Intel® Total Memory Encryption – Multi-Key (Intel® TME-MK)

To better protect computer system memory, the 4th Gen Intel® Xeon® Scalable processor has a security feature called Intel® Total Memory Encryption – Multi-Key (Intel® TME-MK). This feature is supported on the Intel® Server Board M50FCP2SBSTD. Intel® TME-MK helps ensure that all memory accessed from the processors is encrypted, including customer credentials, encryption keys, and other IP or personal information on the external memory bus.

Intel developed this feature to provide greater protection for system memory against hardware attacks, such as removing and reading the dual in-line memory module after spraying it with liquid nitrogen or installing

purpose-built attack hardware. Using the National Institute of Standards and Technology (NIST) storage encryption standard AES XTS, an encryption key is generated using a hardened random number generator in the processor without exposure to software. This approach allows existing software to run unmodified while better protecting memory.

Intel® TME-MK builds on Intel® TME and adds support for multiple encryption keys. The System on Chip (SoC) implementation supports a fixed number of encryption keys. Software can configure the SoC to use a subset of available keys. Software manages the use of keys and can use each of the available keys for encrypting any page of the memory. Thus, Intel® TME-MK allows page granular encryption of memory. Intel® TME-MK can be enabled directly in the server BIOS and is compatible with Intel® SGX application enclave solutions.

Intel® TME-MK has the following characteristics:

- **Encrypts** the memory using a NIST standard "storage-class" algorithm for encryption: AES-XTS.
- **Transparent to software**, it encrypts data before writing to server memory and then decrypts on read.
- **Easy enablement** that requires no operating system or application enabling and is applicable to all operating systems.

To enable/disable Intel® TME-MK, access the BIOS setup utility menu by pressing **<F2>** key during POST. Navigate to the following menu: **Advanced > Processor Configuration**

Important Note: When Intel® TME-MK is enabled, a subset of memory RAS features and Intel® Optane™ PMem 300 series (if installed) is disabled.

For more information on Intel® TME-MK, see the *BIOS Setup Utility User Guide* and the *BIOS Firmware EPS.*

12.5 Intel® Software Guard Extensions (Intel® SGX)

Intel® Software Guard Extensions (Intel® SGX) is a set of instructions that increases the security of application code and data, giving them more protection from disclosure or modification. Developers can partition sensitive information into enclaves that are areas of execution in memory with more security protection.

Intel® SGX helps to protect selected code and data from disclosure or modification. Intel® SGX helps partition applications into enclaves in memory that increase security. Enclaves have hardware-assisted confidentiality and integrity-added protections to help prevent access from processes at higher privilege levels. Through attestation services, a relying party can receive some verification on the identity of an application enclave before launch.

The Intel® Server Board M50FCP2SBSTD provides Intel® SGX. Intel® SGX provides fine grain data protection via application isolation in memory. Data protected includes code, transactions, IDs, keys, key material, private data, algorithms. Intel® SGX provides enhanced security protections for application data independent of operating system or hardware configuration. Intel® SGX provides the following security features:

- **Helps protect against attacks on software,** even if OS/drivers/BIOS/VMM/SMM are compromised.
- **Increases protections for secrets,** even when the attacker has full control of platform.
- **Helps prevent attacks**, such as memory bus snooping, memory tampering, and "cold boot" attacks, against memory contents in RAM.
- **Provides an option for hardware-based attestation** capabilities to measure and verify valid code and data signatures.

Intel® SGX for Intel® Xeon® Scalable processors is optimized to meet the application isolation needs of server systems in cloud environments:

- Massively increased Enclave Cache Page (ECP) size (up to 1 TB for typical dual-socket server system).

- Significant performance improvements: minimal impact vs non-encrypted execution (significantly reduced overhead depending on workload).
- Fully software and binary-compatibility with applications written for other variants of Intel® SGX.
- Support for deployers to control which enclaves can be launched.
- Provides deployers with full control over attestation stack, compatible with Intel® Software Guard Extensions Data Center Attestation Primitives (Intel® SGX DCAP).
- Full protection against cyber (software) attacks, some reduction in protection against physical attacks (no integrity/anti-replay protections) vs other Intel® SGX variants.
- Designed for environments where the physical environment is still trusted.

Note: Intel® SGX can only be enabled when Intel® TME is enabled. See Section 12.4 to enable Intel® TME.

To enable/disable Intel® SGX, access the BIOS setup utility menu by pressing the **<F2>** key during POST. Navigate to the following menu: **Advanced > Processor Configuration**.

Important Note: When Intel® TME-MK is enabled, a subset of memory RAS features and Intel® Optane™ PMem 300 series (if installed) is disabled.

For more information on Intel® SGX, see the *Intel® BIOS Setup Utility User Guide* and the *Intel® BIOS Firmware EPS.*

12.6 Trusted Platform Module (TPM) 2.0 Support

The trusted platform module (TPM) option is a hardware-based security device that addresses the growing concern about boot process integrity and offers better data protection. TPM protects the system startup process by ensuring that it is tamper-free before releasing system control to the operating system. A TPM device provides secured storage to store data, such as security keys and passwords. In addition, a TPM device has encryption and hash functions. The server board implements TPM as per *TPM PC Client Specifications, Revision 2.0,* published by the Trusted Computing Group (TCG).

On the Intel® Server Board M50FCP2SBSTD, a TPM device is installed on to a connector on the server board and is secured using a tamper resistant screw to prevent physical theft and tampering of the device.
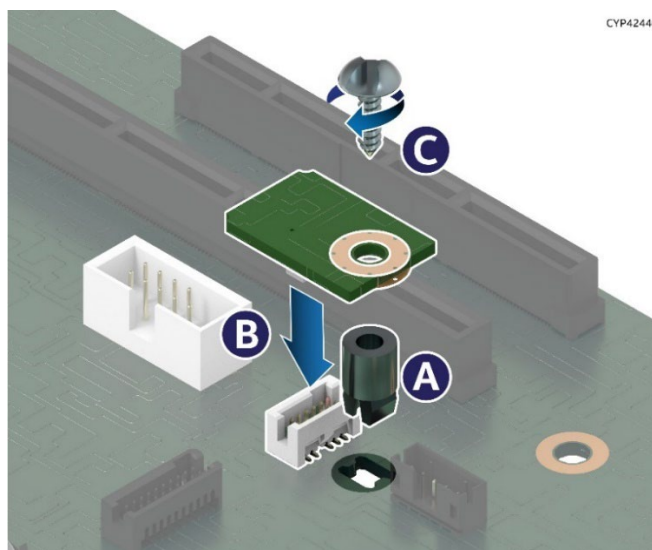
Figure 71. Intel® TPM Module Placement

A pre-boot environment, such as the BIOS and operating system loader, uses the TPM to collect and store unique measurements from multiple factors within the boot process to create a system fingerprint. This unique fingerprint remains the same unless the pre-boot environment is tampered with. Therefore, it is used to compare to future measurements to verify the integrity of the boot process.

After the system BIOS completes the measurement of its boot process, it hands off control to the operating system loader and, in turn, to the operating system. If the operating system is TPM-enabled, it compares the BIOS TPM measurements to those of previous boots to make sure that the system was not tampered with before continuing the operating system boot process. Once the operating system is running, it optionally uses the TPM to provide additional system and data security (for example, BitLocker* drive encryption utility in Microsoft Windows* uses the TPM to store cryptographic keys).

12.6.1   BIOS Support for Trusted Platform Module (TPM)

The BIOS TPM support conforms to the Trusted Computing Group (TCG) PC Client TPM Interface Specification, and the Microsoft Windows* BitLocker* Requirements. The role of the BIOS for TPM security includes the following:

- Measures and stores the finger print of the boot process in the TPM microcontroller allowing a TPM-enabled operating system to verify system boot integrity.
- Provides UEFI compliant APIs to a TPM-enabled operating system for using TPM.
- Generates ACPI table for TPM device allowing a TPM-enabled operating system to administer TPM through the BIOS.
- Verifies operator physical presence.
- Provides BIOS setup options to change TPM security states and to clear TPM ownership.

For additional details, see the *TCG PC Client Specific Implementation Specification*, the *TCG PC Client Specific Physical Presence Interface Specification*, and the *Microsoft Windows* BitLocker* Requirements* documents.

12.6.2   Physical Presence Verification

The operator must confirm TPM ownership by verifying his physical presence before administrative requests to the TPM can be executed. The BIOS implements the operator presence verification by requesting and checking the administrator password. A TPM administrative sequence invoked from the operating system proceeds as follows:

1. A user makes a TPM administrative request through the operating system's security software.
2. The operating system requests the BIOS to execute the TPM administrative command through TPM ACPI methods and then resets the system.
3. The BIOS verifies the physical presence and confirms the command with the operator.
4. The BIOS executes TPM administrative command, inhibits BIOS setup utility entry, and boots directly to the operating system that requested the TPM command.

12.6.3   TPM Security Setup Options

The security page in the BIOS setup utility allows the administrator to view the current TPM state and to carry out rudimentary TPM administrative operations. Performing TPM administrative operations through the BIOS setup utility requires physical presence verification.

The administrator can turn TPM functionality on or off and clear the TPM ownership contents. After the requested BIOS TPM setup operation is carried out, the **TPM2 Operation** field in the BIOS Setup utility reverts to **No Operation**.

The BIOS TPM setup also displays the current state of the TPM, whether TPM is enabled or disabled and activated or deactivated. While using TPM, a TPM-enabled operating system or application may change the TPM state independently of the BIOS setup utility. When an operating system modifies the TPM state, the BIOS setup utility displays the updated TPM state.

The BIOS setup utility **TPM Clear** option allows the operator to clear the TPM ownership key and allows the operator to take control of the system with TPM. You use this option to clear security settings for a newly initialized system or to clear a system for which the TPM ownership security key was lost.

12.7 Converged Intel® Boot Guard and Intel® Trusted Execution Technology (Intel® TXT)

Intel® Boot Guard

- Provides mechanism to authenticate the initial BIOS code, before BIOS starts.
- Hardware-based static root of trust for Measurement (SRTM).
- Defends against attackers replacing or modifying the platform firmware.

Intel® TXT

- Provides the ability to attest the authenticity of a platform configuration and operating system environment; establish trust.
- Hardware-based dynamic root of trust for measurement (DRTM).
- Defends against software-based attacks

Previous generation of Intel® servers supported Intel® Boot Guard and Intel® Trusted Execution Technology (Intel® TXT). The two security technologies combined included some redundancies and inefficiencies between them. With this product generation, Intel® rearchitected and fused together the two technologies into the Intel® CBnT (Converged Intel® Boot Guard and Trusted Execution Technology). Combining the two technologies into one made them more efficient, eliminated redundancies between them, simplified their implementation, and provided stronger protections.

For more information, visit http://www.intel.com/technology/security/.

12.8 Unified Extensible Firmware Interface (UEFI) Secure Boot Technology

UEFI secure boot technology defines how a platform's firmware can authenticate a digitally signed UEFI image, such as an operating system loader or a UEFI driver stored in an option ROM. This provides the capability to ensure that those UEFI images are only loaded in an owner authorized fashion and provides a common means to ensure platform security and integrity over systems running UEFI-based firmware. The BIOS for the Intel® Server Board M50FCP2SBSTD is compliant with the UEFI specifications 2.3.1 Errata C for UEFI secure boot feature.

UEFI secure boot requires native UEFI boot mode, and it disables legacy Option ROM dispatch. By default, secure boot on Intel server boards is disabled.

To enable / disable UEFI Secure Boot in the BIOS setup utility menu, select **Boot Maintenance Manager** > **Advanced Boot Options** > **Secure Boot Configuration**.

For more information on UEFI Secure Boot Technology, see the *BIOS Setup Utility User Guide* and *BIOS Firmware External Product Specification (EPS)*.

13. Server Board Configuration and Service Jumpers

The server board includes several jumper blocks to configure, protect, or recover specific features of the server board. The following figure identifies the location of each jumper block on the server board. Pin 1 of each jumper can be identified by the arrowhead (▼) silkscreened on the server board next to the pin. The following sections describe how each jumper is used.
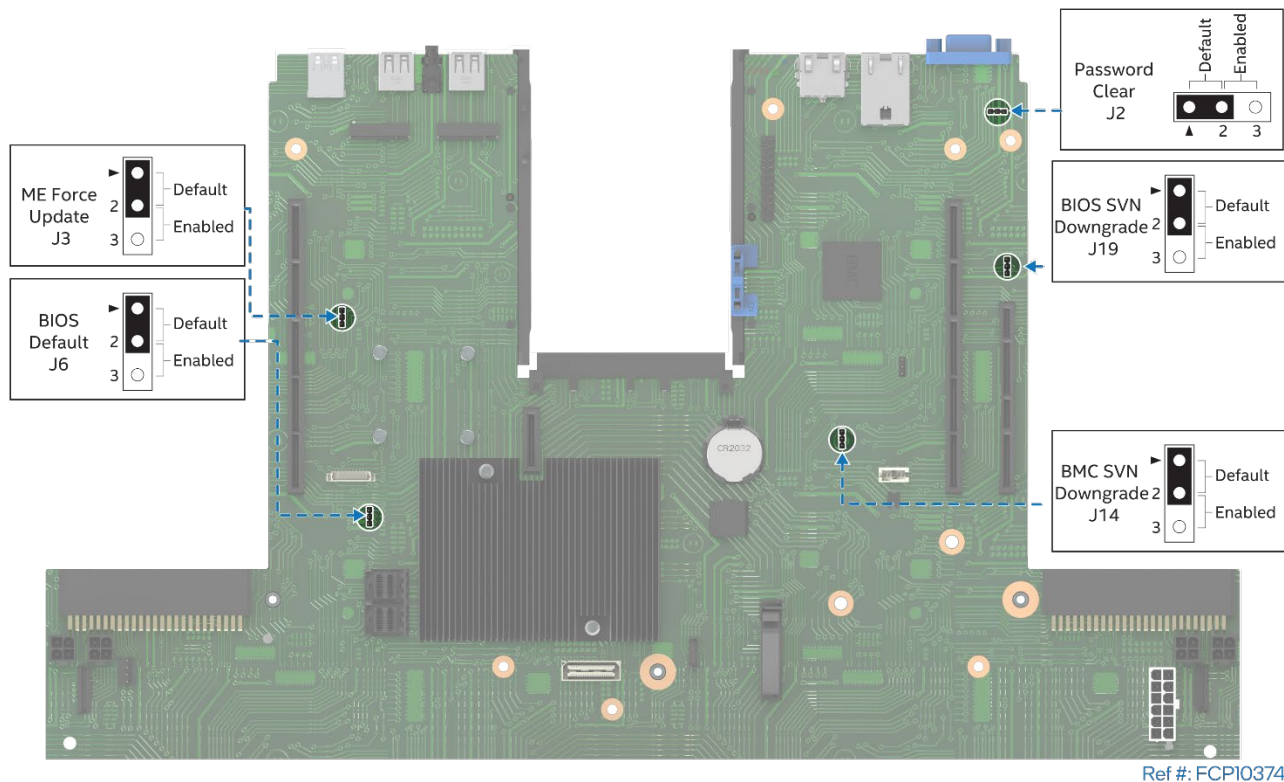
Figure 72. Reset and Recovery Jumper Header Locations

13.1 BIOS Default Jumper (BIOS DFLT – J6)

This jumper resets BIOS options, configured using the <F2> BIOS setup utility, back to their original default factory settings.

Note: This jumper does not reset administrator or user passwords. To reset passwords, the Password Clear jumper must be used.

To use the BIOS default jumper, perform the following steps:

1. Power down the server system
2. Unplug the power cord(s).
3. Remove the system top cover
4. Remove the riser assembly
5. Move the "BIOS DFLT" (J6) jumper from pins 1–2 (normal operation) to pins 2–3 (set BIOS defaults).
6. Wait five seconds, then move the jumper back to pins 1–2.
7. Reinstall the riser assembly
8. Reinstall the system top cover.
9. Reinstall system power cords.

Note: The system automatically powers on after AC power is applied to the system.

10. Press **<F2>** during POST to access the BIOS setup utility and configure and save desired BIOS options.

After resetting BIOS options using the BIOS default jumper, the Error Manager Screen in the BIOS setup utility displays two errors:

- 0012   System RTC date/time not set
- 5220   BIOS settings reset to default settings

The system time and date need to be reset.

13.2 Password Clear Jumper (PASSWD_CLR – J2)

This jumper causes both the user password and the administrator password to be cleared if they were set. The operator should be aware that this situation creates a security gap until passwords have been configured again through the BIOS setup utility. This is the only method by which the administrator and user passwords can be cleared unconditionally. Other than this jumper, passwords can only be set or cleared by changing them explicitly in BIOS setup utility. No method of resetting BIOS configuration settings to default values affects either the administrator or user passwords.

To use the password clear jumper, perform the following steps:

1. Power down the server system.
2. For safety, unplug the power cord(s).
3. Remove the system top cover.
4. Move the "PASSWD_CLR" (J2) jumper from pins 1–2 (default) to pins 2–3 (password clear position).
5. Reinstall the system top cover
6. Reattach the power cord(s).
7. Power up the server and press **<F2>** to access the BIOS setup utility.
8. Verify the password clear operation was successful by viewing the Error Manager screen. Two errors should be logged:
    - o   5221   Passwords cleared by jumper
    - o   5224   Password clear jumper is set
9. Exit the BIOS setup utility and power down the server.
10. For safety, remove the power cord(s)
11. Remove the system top cover.
12. Move the "PASSWD_CLR" (J2) jumper back to pins 1–2 (default).
13. Reinstall the system top cover
14. Reattach the power cord(s).
15. Power up the server system.
16. Intel strongly recommends booting into the <F2> BIOS setup utility immediately, navigate to the Security tab, and set the administrator and user passwords if intending to use BIOS password protection.

13.3 Intel® Management Engine (Intel® ME) Firmware Force Update Jumper (ME_FRC_UPDT – J3)

When the Intel® ME firmware force update jumper is moved from its default position, the Intel® ME is forced to operate in a reduced operating capacity. This jumper should only be used if the Intel® ME firmware has gotten corrupted and requires reinstallation.

Note: The Intel® ME image file is included in the system update packages (SUP) posted to Intel's download center website at http://downloadcenter.intel.com.

To use the Intel® ME firmware force update jumper, perform the following steps:

1. Turn off the system and detach all power cords

Note: If the Intel® ME force update jumper is moved with power connected to the system, the Intel® ME will not operate properly.

2. Remove any chassis panels needed to access the inside of the server system.
3. Remove or move aside any installed system components blocking access to the ME Force Update jumper (J3) jumper
4. Move the ME Force Update jumper (J3) jumper from pins 1–2 (default) to pins 2–3 (force update position)
5. Reinstall any removed system components (if needed).
6. Reattach the power cord(s) and power on the system
7. Boot to the EFI shell and update the Intel® ME firmware following the instructions provided with the system update package
8. When the update has successfully completed, power off the system and detach all power cords
9. Remove any chassis panels needed to access the inside of the server system.
10. Remove or move aside any installed system components blocking access to the ME Force Update jumper (J3) jumper
11. Move the ME Force Update jumper (J3) jumper back to pins 1–2 (default).
12. Reinstall any removed system components (if needed).
13. Reattach the power cord(s)
14. Power on the system

13.4 BIOS Security Version Number (SVN) Downgrade Jumper (BIOS_SVN_DG – J19)

The BIOS SVN Downgrade jumper is labeled **SNV_BYPASS** on the server board. When this jumper is moved from its default pin position (pins 1–2), it allows the server system firmware (including BIOS) in the PFR-controlled PCH capsule file to be downgraded to a previous revision.

Caution: Downgrading to an older version of BIOS may result in the loss of functionality and security features that are present in a later version but was not implemented in the older version.

Caution: When downgrading to an older version of BIOS, server systems may end up with a firmware stack combination that is not supported, and therefore could experience unpredictable behavior.

Note: Latest system update packages are included in the SUP posted to Intel's download center website at http://downloadcenter.intel.com.

To use the BIOS SVN Downgrade jumper, perform the following steps:

1. Power off the system.
2. Remove any chassis panels needed to access the inside of the server system.
3. Remove or move aside any installed system components blocking access to the BIOS SVN Downgrade jumper block (J19).
4. Move the BIOS SVN Downgrade jumper (J19) jumper from pins 1–2 (default) to pins 2–3 (SVN Bypass).
5. Reinstall any removed system components (if needed).
6. Power on the system. The system automatically boots to the EFI shell.
7. Update the BIOS using the standard update instructions provided with the system update package.
8. After the BIOS update has successfully completed, repeat steps 1 thru 3 and proceed to Step 9.
9. Move the BIOS SVN Downgrade jumper (J19) jumper back to pins 1–2 (default).
10. Reinstall any removed system components (if needed).
11. Power on the system. During POST, press **<F2>** to access the BIOS setup utility to configure and save desired BIOS options.

13.5 BMC Security Version Number (SVN) Downgrade Jumper (BMC_SVN_DG – J14)

When BMC SVN Downgrade jumper is moved from its default pin position (pin 1–2) to the pin 2–3 position, it allows the system BMC firmware in the PFR-controlled BMC capsule file to be downgraded to a lower Security Version Number (SVN).

Caution: Downgrading to a BMC version with lower SVN may result in the loss of functionality and security features that are present in a higher SVN but were not implemented in the lower SVN.

Caution: When downgrading to an older version of BMC, modules may end up with a firmware stack combination that is not supported, and therefore could experience unpredictable behavior.

Note: Latest system update packages are included in the SUP posted to Intel's download center website at http://downloadcenter.intel.com.

To use the BMC_SVN_DG Downgrade jumper, perform the following steps:

1. Power off the system.
2. Remove any chassis panels needed to access the inside of the server system.
3. Remove or move aside any installed system components blocking access to the BMC SVN Downgrade jumper (J14).
4. Move the BMC SVN Downgrade jumper (J14) from pins 1–2 (default) to pins 2–3 (enabled).
5. Reinstall any removed system components (if needed).
6. Power on the system. The system automatically boots to the EFI shell.
7. Update the BMC using the standard update instructions provided with the system update package.
8. After the BMC update has successfully completed, repeat Steps 1 thru 3, then proceed to Step 9.
9. Move the BMC SVN Downgrade jumper (J14) back to pins 1–2 (default).
10. Reinstall any removed system components (if needed).
11. Power on the system.

Appendix A. Getting Help

Available Intel® support options with your Intel® Server System:

1. 24x7 support through Intel's support webpage at https://www.intel.com/content/www/us/en/support/products/1201/server-products.html

    Information available at the support site includes:

    - Latest BIOS, firmware, drivers, and utilities
    - Product documentation, setup, and service guides
    - Full product specifications, technical advisories, and errata
    - Compatibility documentation for memory, hardware add-in cards, and operating systems
    - Server and chassis accessory parts list for ordering upgrades or spare parts
    - A searchable knowledge base to search for product information throughout the support site

    Quick Links:

Use the following links for support on Intel® Server Boards and Server Systems	**Download Center**	**BIOS Support Page**	**Troubleshooting Boot Issue**
	http://www.intel.com/support/downloadserversw	http://www.intel.com/support/serverbios	http://www.intel.com/support/tsboot
Use the following links for support on Intel® Data Center Block (DCB) Integrated Systems* * Intel® DCB comes pre-populated with processors, memory, storage, and peripherals based on how it was ordered through the Intel® Configure to Order tool.	**Download Center** http://www.intel.com/support/downloaddcbsw	**Technical Support Documents** http://www.intel.com/support/dcb	**Warranty and Support Info** http://www.intel.com/support/dcbwarranty

2. If a solution cannot be found at Intel's support site, submit a service request via Intel's online service center at https://supporttickets.intel.com/servicecenter?lang=en-US . In addition, you can also view previous support requests. (Login required to access previous support requests)

3. Contact an Intel® support representative using one of the support phone numbers available at https://www.intel.com/content/www/us/en/support/contact-support.html (charges may apply).

Intel® also offers the Intel® Partner Alliance program members around-the-clock 24x7 technical phone support on Intel® server boards, server chassis, server RAID controller cards, and Intel® Server Management at https://www.intel.com/content/www/us/en/partner-alliance/overview.html.

Note: The 24x7 support number is available after logging in to the Intel® Partner Alliance website.

Warranty Information

To obtain warranty information, visit http://www.intel.com/p/en_US/support/warranty.

Appendix B. Integration and Usage Tips

This appendix provides a list of useful information that is unique to the Intel® Server Board M50FCP2SBSTD and should be kept in mind while configuring your server system.

- When adding or removing components or peripherals from the server board, power cords must be disconnected from the server. With power applied to the server, standby voltages are still present even though the server board is powered off.

- The server board supports the 4th Gen Intel® Xeon® Scalable processor family with a Thermal Design Power (TDP) of up to and including 350 Watts. Previous generations of the Intel® Xeon® processor and Intel® Xeon® Scalable processor families are not supported. Server systems using these server boards may or may not meet the TDP design limits of the server board. Validate the TDP limits of the server system before selecting a processor.

- Processors must be installed in order. CPU 0 must be populated for the server board to operate.

- Riser Card Slots #2 and #3 on the server board can only be used in dual processor configurations.

- The riser card slots are specifically designed to support riser cards only. Attempting to install a PCIe add-in card directly into a riser card slot on the server board may damage the server board, the add-in card, or both.

- For best performance, the number of DDR5 DIMMs installed should be balanced across both processor sockets and memory channels.

- On the back edge of the server board, are eight POST Code Diagnostic LEDs that display a sequence of POST codes during the boot process. If the server board hangs during POST, the LEDs display the last POST event run before the hang.

- The system status LED is set to a steady amber color for all fatal errors that are detected during processor initialization. A steady amber system status LED indicates that an unrecoverable system failure condition has occurred.

- Ensure that the latest system software is loaded on the server. This includes system BIOS, BMC firmware, and Intel® ME firmware. The latest system software can be downloaded from http://downloadcenter.intel.com.

Appendix C. Post Code Diagnostic LED Decoder

As an aid in troubleshooting a system hang that occurs during system POST execution, the server board includes a bank of eight (2X4) diagnostic LEDs on the back edge of the board. These diagnostic LEDs are used during POST to represent POST progress codes or halt error codes.

During the system boot process, Memory Reference Code (MRC) and system BIOS execute several memory initialization and platform configuration routines, each of which is assigned a hexadecimal POST progress code number. As each routine is started, the given POST progress code number is displayed on the POST Code Diagnostic LEDs.

If a system hangs during POST execution, the displayed POST progress code can be used to identify the last POST routine that was run before the error occurred, helping to isolate the possible cause of the hang condition even when video is not available.

These diagnostic LEDs are equivalent to the legacy "Port 80 POST Codes", and a Legacy I/O Port 80 output will be displayed as a Diagnostic LED code. Each POST progress code or halt error code is represented by eight LEDs; four green LEDs and four amber LEDs. The codes are divided into two nibbles, an upper nibble, and a lower nibble. The upper nibble bits are represented by amber diagnostic LEDs and the lower nibble bits are represented by green diagnostics LEDs. If the bit is set, the corresponding LED is lit. If the bit is clear, the corresponding LED is off. For each set of nibble bits, LED 0 represents the least significant bit (LSB) and LED 3 represents the most significant bit (MSB).
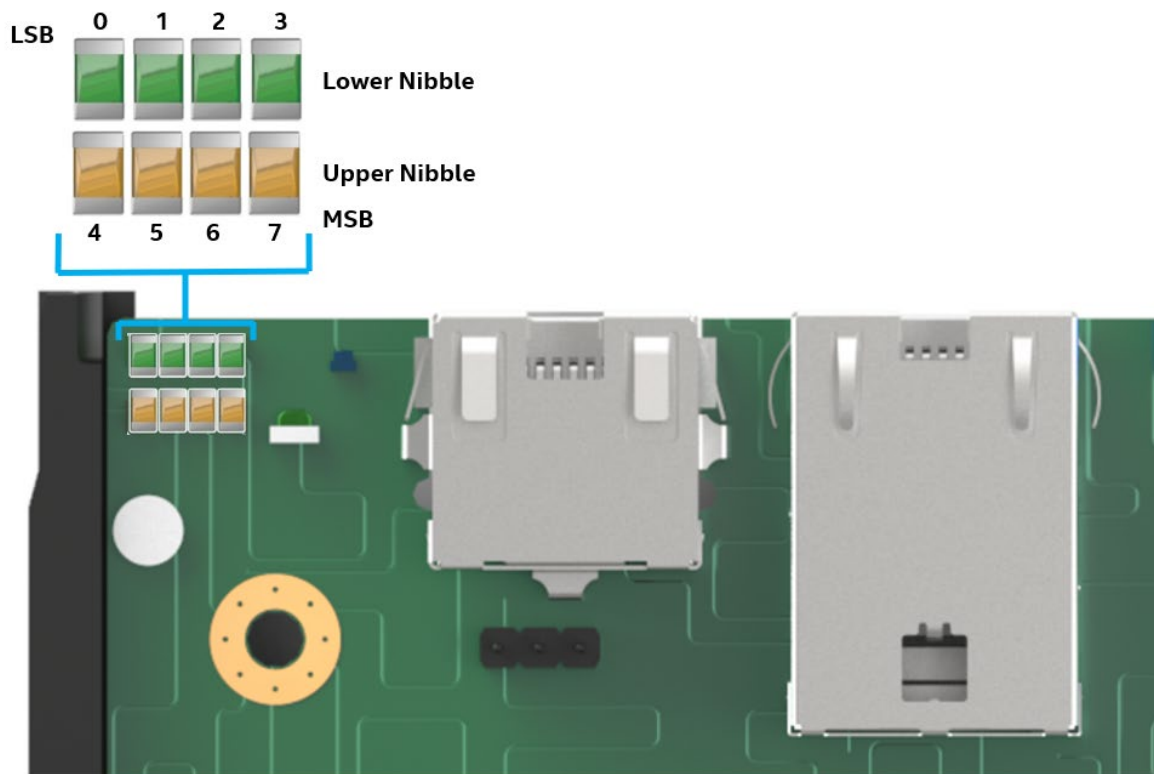
Figure 73. Server Board POST Diagnostic LEDs

Note: Diagnostic LEDs are best read and decoded when viewing the LEDs from the back of the system with the four amber LEDs read and decoded first (MSB to LSB), followed by the four green LEDs (MSB to LSB).

In the following example, the BIOS sends a hex value of "**AC"** to the diagnostic LEDs. The LEDs are decoded as shown in the following table.

Table 58. POST Progress Code LED Example

LEDs		Upper Nibble AMBER LEDs				Lower Nibble GREEN LEDs			
		MSB							LSB
		LED #7	LED #6	LED #5	LED #4	LED #3	LED #2	LED #1	LED #0
		8h	4h	2h	1h	8h	4h	2h	1h
Status		ON	OFF	ON	OFF	ON	ON	OFF	OFF
Read Value	Binary	1	0	1	0	1	1	0	0
	Hexadecimal	Ah				Ch			
Result		ACh							

Note: Upper nibble bits = 1010b = Ah; Lower nibble bits = 1100b = Ch; the two Hex Nibble values are combined to create a single ACh POST Progress Code.

C.1   Early POST Memory Initialization MRC Diagnostic Codes

Memory initialization at the beginning of POST includes multiple functions: discovery, channel training, validation that the memory module population is acceptable and functional, initialization of the IMC and other hardware settings, and initialization of applicable RAS configurations.

The MRC progress codes are displayed on the diagnostic LEDs that show the execution point in the MRC operational path at each step.

Table 59. Memory Reference Code (MRC) Progress Codes

MRC Progress Code (Hex)	Upper Nibble				Lower Nibble				Description
	8h	4h	2h	1h	8h	4h	2h	1h	
73	0	1	1	1	0	0	1	1	NVRAM sync.
7E	0	1	1	1	1	1	1	0	MRC internal sync.
B0	1	0	1	1	0	0	0	0	Detect DIMM population
B1	1	0	1	1	0	0	0	1	Set DDR5 frequency
B2	1	0	1	1	0	0	1	0	Gather remaining SPD data
B3	1	0	1	1	0	0	1	1	Program registers on the memory controller level
B4	1	0	1	1	0	1	0	0	Evaluate RAS modes and save rank information
B5	1	0	1	1	0	1	0	1	Program registers on the channel level
B6	1	0	1	1	0	1	1	0	Perform the JEDEC defined initialization sequence
B7	1	0	1	1	0	1	1	1	Train DDR5 ranks
0	0	0	0	0	0	0	0	0	Train DDR5 channels: Receive enable training
3	0	0	0	0	0	0	1	1	Train DDR5 channels: Read DQ/DQS training
4	0	0	0	0	0	1	0	0	Train DDR5 channels: Write DQ/DQS training
11	0	0	0	1	0	0	0	1	Train DDR5 channels: End of channel training.
77	0	1	1	1	0	1	1	1	Train DDR5 channels: Write leveling training.
B8	1	0	1	1	1	0	0	0	Initialize CLTT/OLTT
B9	1	0	1	1	1	0	0	1	Hardware memory test and initialization
BA	1	0	1	1	1	0	1	0	Execute software memory initialization
BB	1	0	1	1	1	0	1	1	Program memory map and interleaving
BC	1	0	1	1	1	1	0	0	Program RAS configuration

MRC Progress Code (Hex)	Upper Nibble				Lower Nibble				Description
	8h	4h	2h	1h	8h	4h	2h	1h	
BE	1	0	1	1	1	1	1	0	Execute BSSA RMT
BF	1	0	1	1	1	1	1	1	MRC is done

If a major memory initialization error occurs, preventing the system from booting with data integrity, a beep code is generated, the MRC displays a fatal error code on the diagnostic LEDs, and a system halt command is executed. Fatal MRC error halts do not change the state of the system status LED and they do not get logged as SEL events. Table 60 lists all MRC fatal errors that are displayed to the diagnostic LEDs.

Note: Fatal MRC error codes may be the same as BIOS POST progress codes displayed later in the POST process. The fatal MRC error codes can be distinguished from the BIOS POST progress codes by the accompanying memory failure beep code of three long beeps. All MRC error codes are identified in Table 60.

Table 60. MRC Fatal Error Codes

MRC Fatal Error Code (Hex)	Upper Nibble				Lower Nibble				Description
	8h	4h	2h	1h	8h	4h	2h	1h	
E8	1	1	1	0	1	0	0	0	No usable memory error 01h = No memory was detected from SPD read, or invalid config that causes no operable memory. 02h = Memory DIMMs on all channels of all sockets are disabled due to hardware memory test error. 03h = No memory installed. All channels are disabled.
E9	1	1	1	0	1	0	0	1	Memory is locked by Intel® TXT and is inaccessible
EA	1	1	1	0	1	0	1	0	DDR5 channel training error 01h = Error on read DQ/DQS (Data/Data Strobe) initialization 02h = Error on Receive Enable 03h = Error on Write Leveling 04h = Error on write DQ/DQS (Data/Data Strobe)
EB	1	1	1	0	1	0	1	1	Memory test failure 01h = Software memory test failure. 02h = Hardware memory test failed.
ED	1	1	1	0	1	1	0	1	DIMM configuration population error 01h = Different DIMM types (RDIMM, 3DS-RDIMM) are detected installed in the system. 02h = Violation of DIMM population rules. 03h = The 3rd DIMM slot cannot be populated when QR DIMMs are installed. 04h = UDIMMs are not supported. 05h = Unsupported DIMM Voltage.
EF	1	1	1	0	1	1	1	1	Indicates a CLTT table structure error

C.2 BIOS POST Progress Codes

The following table provides a list of all POST progress codes.

Table 61. POST Progress Codes

Post progress code (Hex)	Upper Nibble				Lower Nibble				Description
	8h	4h	2h	1h	8h	4h	2h	1h	
Security (SEC) Phase									
01	0	0	0	0	0	0	0	1	First POST code after CPU reset
02	0	0	0	0	0	0	1	0	Microcode load begins
03	0	0	0	0	0	0	1	1	CRAM initialization begins
04	0	0	0	0	0	1	0	0	PEI cache when disabled
05	0	0	0	0	0	1	0	1	SEC core at power-on start
06	0	0	0	0	0	1	1	0	Early CPU initialization during SEC phase
Intel® UPI RC (fully leverage without platform change)									
A1	1	0	1	0	0	0	0	1	Collect information such as SBSP, boot mode, reset type, etc.
A3	1	0	1	0	0	0	1	1	Setup minimum path between SBSP and other sockets
A6	1	0	1	0	0	1	1	0	Sync up with PBSPs
A7	1	0	1	0	0	1	1	1	Topology discovery and route calculation
A8	1	0	1	0	1	0	0	0	Program final route
A9	1	0	1	0	1	0	0	1	Program final IO SAD setting
AA	1	0	1	0	1	0	1	0	Protocol layer and other uncore settings
AB	1	0	1	0	1	0	1	1	Transition links to full speed operation
AE	1	0	1	0	1	1	1	0	Coherency settings
AF	1	0	1	0	1	1	1	1	Intel® UPI initialization is done
Pre-EFI Initialization (PEI) Phase									
10	0	0	0	1	0	0	0	0	PEI core
11	0	0	0	1	0	0	0	1	CPU PEIM
15	0	0	0	1	0	1	0	1	Platform type initialization
19	0	0	0	1	1	0	0	1	Platform PEIM initialization
Integrated I/O (IIO) Progress Codes									
E0	1	1	1	0	0	0	0	0	IIO early initialization entry
E1	1	1	1	0	0	0	0	1	IIO pre-link training
E2	1	1	1	0	0		1	0	IIO EQ programming
E3	1	1	1	0	0	0	1	1	IIO link training
E4	1	1	1	0	0	1	0	0	Internal use
E5	1	1	1	0	0	1	0	1	IIO early initialization exit
E6	1	1	1	0	0	1	1	0	IIO late initialization entry
E7	1	1	1	0	0	1	1	1	IIO PCIe* ports initialization
E8	1	1	1	0	1	0	0	0	IIO IOAPIC initialization
E9	1	1	1	0	1	0	0	1	IIO VTD initialization
EA	1	1	1	0	1	0	1	0	IIO IOAT initialization
EB	1	1	1	0	1	0	1	1	IIO DXF initialization
EC	1	1	1	0	1	1	0	0	IIO NTB initialization
ED	1	1	1	0	1	1	0	1	IIO security initialization
EE	1	1	1	0	1	1	1	0	IIO late initialization exit
EF	1	1	1	0	1	1	1	1	IIO ready to boot

Post progress code (Hex)	Upper Nibble				Lower Nibble				Description
	8h	4h	2h	1h	8h	4h	2h	1h	
MRC Progress Codes – At this point, the MRC progress code sequence is executed									
31	0	0	1	1	0	0	0	1	Memory installed
32	0	0	1	1	0	0	1	0	CPU PEIM (CPU initialization)
33	0	0	1	1	0	0	1	1	CPU PEIM (cache initialization)
34	0	0	1	1	0	1	0	0	CPU BSP select
35	0	0	1	1	0	1	0	1	CPU AP initialization
36	0	0	1	1	0	1	1	0	CPU SMM initialization
4F	0	1	0	0	1	1	1	1	DXE IPL started
Memory Feature Progress Codes									
C1	1	1	0	0	0	0	0	1	Memory POR check
C2	1	1	0	0	0	0	1	0	Internal use
C3	1	1	0	0	0	0	1	1	Internal use
C4	1	1	0	0	0	1	0	0	Internal use
C5	1	1	0	0	0	1	0	1	Memory early initialization
C6	1	1	0	0	0	1	1	0	Display DIMM information in debug mode
C7	1	1	0	0	0	1	1	1	JEDEC NVDIMM training
C9	1	1	0	0	1	0	0	1	Setup SVL and scrambling
CA	1	1	0	0	1	0	1	0	Internal use
CB	1	1	0	0	1	0	1	1	Check RAS support
CC	1	1	0	0	1	1	0	0	PMem ADR initialization
CD	1	1	0	0	1	1	0	1	Internal use
CE	1	1	0	0	1	1	1	0	Memory late initialization
CF	1	1	0	0	1	1	1	1	Determine MRC boot mode
D0	1	1	0	1	0	0	0	0	MKTME early initialization
D1	1	1	0	1	0	0	0	1	SGX early initialization
D2	1	1	0	1	0	0	1	0	Memory margin test
D3	1	1	0	1	0	0	1	1	Internal use
D5	1	1	0	1	0	1	0	1	Internal use
D6	1	1	0	1	0	1	1	0	Offset training result
Driver Execution Environment (DXE) Phase									
60	0	1	1	0	0	0	0	0	DXE core started
62	0	1	1	0	0	0	1	0	DXE setup initialization
68	0	1	1	0	1	0	0	0	DXE PCI host bridge initialization
69	0	1	1	0	1	0	0	1	DXE NB initialization
6A	0	1	1	0	1	0	1	0	DXE NB SMM initialization
70	0	1	1	1	0	0	0	0	DXE SB initialization
71	0	1	1	1	0	0	0	1	DXE SB SMM initialization
72	0	1	1	1	0	0	1	0	DXE SB devices initialization
78	0	1	1	1	1	0	0	0	DXE ACPI initialization
79	0	1	1	1	1	0	0	1	DXE CSM initialization
7D	0	1	1	1	1	1	0	1	DXE removable media detect
7E	0	1	1	1	1	1	1	0	DXE removable media detected
90	1	0	0	1	0	0	0	0	DXE BDS started
91	1	0	0	1	0	0	0	1	DXE BDS connect drivers

Post progress code (Hex)	Upper Nibble				Lower Nibble				Description
	8h	4h	2h	1h	8h	4h	2h	1h	
92	1	0	0	1	0	0	1	0	DXE PCI bus start
93	1	0	0	1	0	0	1	1	DXE PCI bus HPC initialization
94	1	0	0	1	0	1	0	0	DXE PCI bus enumeration
95	1	0	0	1	0	1	0	1	DXE PCI bus resource requested
96	1	0	0	1	0	1	1	0	DXE PCI bus assign resource
97	1	0	0	1	0	1	1	1	DXE CON_OUT connect
98	1	0	0	1	1	0	0	0	DXE CON_IN connect
99	1	0	0	1	1	0	0	1	DXE SIO initialization
9A	1	0	0	1	1	0	1	0	DXE USB start
9B	1	0	0	1	1	0	1	1	DXE USB reset
9C	1	0	0	1	1	1	0	0	DXE USB detected
9D	1	0	0	1	1	1	0	1	DXE USB enabled
A1	1	0	1	0	0	0	0	1	DXE IDE start
A2	1	0	1	0	0	0	1	0	DXE IDE reset
A3	1	0	1	0	0	0	1	1	DXE IDE detected
A4	1	0	1	0	0	1	0	0	DXE IDE enabled
A5	1	0	1	0	0	1	0	1	DXE SCSI start
A6	1	0	1	0	0	1	1	0	DXE SCSI reset
A7	1	0	1	0	0	1	1	1	DXE SCSI detected
A8	1	0	1	0	1	0	0	0	DXE SCSI enabled
AB	1	0	1	0	1	0	1	1	DXE SETUP start
AC	1	0	1	0	1	1	0	0	DXE SETUP input wait
AD	1	0	1	0	1	1	0	1	DXE ready to boot
AE	1	0	1	0	1	1	1	0	DXE legacy boot
AF	1	0	1	0	1	1	1	1	DXE exit boot services
B0	1	0	1	1	0	0	0	0	RT set virtual address map start
B1	1	0	1	1	0	0	0	1	RT set virtual address map end
B2	1	0	1	1	0	0	1	0	DXE legacy option ROM initialization
B3	1	0	1	1	0	0	1	1	DXE reset system
B4	1	0	1	1	0	1	0	0	DXE USB hot plug
B5	1	0	1	1	0	1	0	1	DXE PCI bus hot plug
B8	1	0	1	1	1	0	0	0	PWRBTN shutdown
B9	1	0	1	1	1	0	0	1	SLEEP shutdown
C0	1	1	0	0	0	0	0	0	End of DXE
C7	1	1	0	0	0	1	1	1	DXE ACPI enable
0	0	0	0	0	0	0	0	0	Clear POST code
BDS Phase									
51	0	1	0	1	0	0	0	1	BDS select video.
52	0	1	0	1	0	0	1	0	BDS after trust console.
53	0	1	0	1	0	0	1	1	BDS end of DXE.
54	0	1	0	1	0	1	0	0	BDS ready to lock.
55	0	1	0	1	0	1	0	1	BDS connect device.
56	0	1	0	1	0	1	1	0	BDS before enter setup.
57	0	1	0	1	0	1	1	1	BDS load boot options.

Post progress code (Hex)	Upper Nibble				Lower Nibble				Description
	8h	4h	2h	1h	8h	4h	2h	1h	
58	0	1	0	1	1	0	0	0	BDS exit boot services.
S3 Resume									
E0	1	1	1	0	0	0	0	0	S3 resume PEIM (S3 started)
E1	1	1	1	0	0	0	0	1	S3 resume PEIM (S3 boot script)
E2	1	1	1	0	0	0	1	0	S3 resume PEIM (S3 video repost)
E3	1	1	1	0	0	0	1	1	S3 resume PEIM (S3 operating system wake)

Appendix D. Post Error Codes

Most error conditions encountered during POST are reported using POST error codes. These codes represent specific failures, warnings, or information. POST error codes may be displayed in the Error Manager display screen in the BIOS Setup utility and are always logged to the System Event Log (SEL). Logged events are available to system management applications, including remote and Out of Band (OOB) management.

There are exception cases in early initialization where system resources are not adequately initialized for handling POST Error Code reporting. These cases are primarily fatal error conditions resulting from initialization of processors and memory, and they are handed by a diagnostic LED display with a system halt.

Table 62 lists the supported POST error codes. Each error code is assigned an error severity that determines the action the BIOS takes when the error is encountered. Error severities include minor, major, and fatal. The BIOS action for each is defined as follows:

- **Minor:** An error message may be displayed on the screen in the BIOS Setup utility Error Manager and the POST error code is logged to the SEL. The system continues booting in a degraded state. The user may want to replace the erroneous unit. The "POST Error Pause" option setting in the BIOS Setup utility does not have an effect on this error.

- **Major:** An error message is displayed on Error Manager screen in the BIOS Setup utility and an error is logged to the SEL. If the BIOS setup option "Post Error Pause" is enabled, operator intervention is required to continue booting the system. If the BIOS setup option "POST Error Pause" is disabled, the system continues to boot.

  Note: For 0048 "Password check failed", the system halts and then, after the next reset/reboot, displays the error code on the Error Manager screen.

- **Fatal**: If the system cannot boot, POST halts the system and displays the following message:

  ```
  Unrecoverable fatal error found. System will not boot until the error is
  resolved
  Press <F2> to enter setup
  ```

  When the **<F2>** key on the keyboard is pressed, the error message is displayed on the Error Manager screen, and an error is logged to the system event log (SEL) with the POST error code. The system cannot boot unless the error is resolved. The faulty component must be replaced. The "POST Error Pause" option setting in the BIOS Setup utility does not have any effect on this error.

Note: The POST error codes in the following table are common to all current generation Intel® server platforms. Features present on a given server board/system determine which of the listed error codes are supported.

Table 62. POST Error Codes, Messages, and Corrective Actions

POST Error Code	Error Message	Corrective Action	Type
0012	System RTC date/time not set		Major
0048	Password check failed	Put right password.	Major
0140	PCI component encountered a PERR error		Major
0141	PCI resource conflict		Major
0146	PCI out of resources error	Enable Memory Mapped I/O above 4 GB item at SETUP to use 64-bit MMIO.	Major
0191	Processor core/thread count mismatch detected	Use identical CPU type.	Fatal
0192	Processor cache size mismatch detected	Use identical CPU type.	Fatal
0194	Processor family mismatch detected	Use identical CPU type.	Fatal
0195	Processor Intel(R) UPI link frequencies unable to synchronize		Fatal
0196	Processor model mismatch detected	Use identical CPU type.	Fatal
0197	Processor frequencies unable to synchronize	Use identical CPU type.	Fatal
5220	BIOS settings reset to default settings		Major
5221	Passwords cleared by jumper		Major
5224	Password clear jumper is Set	Recommend reminding user to install BIOS password as BIOS administrator password is the primary keys for several BIOS security features.	Major
8130	CPU 0 disabled		Major
8131	CPU 1 disabled		Major
8160	CPU 0 unable to apply microcode update		Major
8161	CPU 1 unable to apply microcode update		Major
8170	CPU 0 failed Self-Test (BIST)		Major
8171	CPU 1 failed Self-Test (BIST)		Major
8180	CPU 0 microcode update not found		Minor
8181	CPU 1 microcode update not found		Minor
8190	Watchdog timer failed on last boot.		Major
8198	OS boot watchdog timer failure.		Major
8300	Baseboard Management Controller failed self-test.		Major
8305	Hot Swap Controller failure		Major
83A0	Management Engine (ME) failed self-test.		Major
83A1	Management Engine (ME) Failed to respond.		Major
84F2	Baseboard management controller failed to respond		Major
84F3	Baseboard Management Controller in Update Mode.		Major
84F4	Baseboard Management Controller Sensor Data Record empty.	Update right SDR.	Major
84FF	System Event Log full	Clear SEL through EWS or SELVIEW utility.	Minor
85FC	Memory component could not be configured in the selected RAS mode		Major
8501	Memory Population Error	Plug DIMM at right population.	Major
8502	PMem invalid DIMM population found on the system.	Populate valid POR PMem DIMM population.	Major
8520	Memory failed test/initialization CPU0_DIMM_A1	Remove the disabled DIMM.	Major
8521	Memory failed test/initialization CPU0_DIMM_A2	Remove the disabled DIMM.	Major

POST Error Code	Error Message	Corrective Action	Type
8522	Memory failed test/initialization CPU0_DIMM_A3	Remove the disabled DIMM.	Major
8523	Memory failed test/initialization CPU0_DIMM_B1	Remove the disabled DIMM.	Major
8524	Memory failed test/initialization CPU0_DIMM_B2	Remove the disabled DIMM.	Major
8525	Memory failed test/initialization CPU0_DIMM_B3	Remove the disabled DIMM.	Major
8526	Memory failed test/initialization CPU0_DIMM_C1	Remove the disabled DIMM.	Major
8527	Memory failed test/initialization CPU0_DIMM_C2	Remove the disabled DIMM.	Major
8528	Memory failed test/initialization CPU0_DIMM_C3	Remove the disabled DIMM.	Major
8529	Memory failed test/initialization CPU0_DIMM_D1	Remove the disabled DIMM.	Major
852A	Memory failed test/initialization CPU0_DIMM_D2	Remove the disabled DIMM.	Major
852B	Memory failed test/initialization CPU0_DIMM_D3	Remove the disabled DIMM.	Major
852C	Memory failed test/initialization CPU0_DIMM_E1	Remove the disabled DIMM.	Major
852D	Memory failed test/initialization CPU0_DIMM_E2	Remove the disabled DIMM.	Major
852E	Memory failed test/initialization CPU0_DIMM_E3	Remove the disabled DIMM.	Major
852F	Memory failed test/initialization CPU0_DIMM_F1	Remove the disabled DIMM.	Major
8530	Memory failed test/initialization CPU0_DIMM_F2	Remove the disabled DIMM.	Major
8531	Memory failed test/initialization CPU0_DIMM_F3	Remove the disabled DIMM.	Major
8532	Memory failed test/initialization CPU0_DIMM_G1	Remove the disabled DIMM.	Major
8533	Memory failed test/initialization CPU0_DIMM_G2	Remove the disabled DIMM.	Major
8534	Memory failed test/initialization CPU0_DIMM_G3	Remove the disabled DIMM.	Major
8535	Memory failed test/initialization CPU0_DIMM_H1	Remove the disabled DIMM.	Major
8536	Memory failed test/initialization CPU0_DIMM_H2	Remove the disabled DIMM.	Major
8537	Memory failed test/initialization CPU0_DIMM_H3	Remove the disabled DIMM.	Major
8538	Memory failed test/initialization CPU1_DIMM_A1	Remove the disabled DIMM.	Major
8539	Memory failed test/initialization CPU1_DIMM_A2	Remove the disabled DIMM.	Major
853A	Memory failed test/initialization CPU1_DIMM_A3	Remove the disabled DIMM.	Major
853B	Memory failed test/initialization CPU1_DIMM_B1	Remove the disabled DIMM.	Major
853C	Memory failed test/initialization CPU1_DIMM_B2	Remove the disabled DIMM.	Major
853D	Memory failed test/initialization CPU1_DIMM_B3	Remove the disabled DIMM.	Major
853E	Memory failed test/initialization CPU1_DIMM_C1	Remove the disabled DIMM.	Major
853F (Go to 85C0)	Memory failed test/initialization CPU1_DIMM_C2	Remove the disabled DIMM.	Major
8540	Memory disabled.CPU0_DIMM_A1	Remove the disabled DIMM.	Major
8541	Memory disabled.CPU0_DIMM_A2	Remove the disabled DIMM.	Major
8542	Memory disabled.CPU0_DIMM_A3	Remove the disabled DIMM.	Major
8543	Memory disabled.CPU0_DIMM_B1	Remove the disabled DIMM.	Major
8544	Memory disabled.CPU0_DIMM_B2	Remove the disabled DIMM.	Major
8545	Memory disabled.CPU0_DIMM_B3	Remove the disabled DIMM.	Major
8546	Memory disabled.CPU0_DIMM_C1	Remove the disabled DIMM.	Major
8547	Memory disabled.CPU0_DIMM_C2	Remove the disabled DIMM.	Major
8548	Memory disabled.CPU0_DIMM_C3	Remove the disabled DIMM.	Major
8549	Memory disabled.CPU0_DIMM_D1	Remove the disabled DIMM.	Major
854A	Memory disabled.CPU0_DIMM_D2	Remove the disabled DIMM.	Major
854B	Memory disabled.CPU0_DIMM_D3	Remove the disabled DIMM.	Major
854C	Memory disabled.CPU0_DIMM_E1	Remove the disabled DIMM.	Major
854D	Memory disabled.CPU0_DIMM_E2	Remove the disabled DIMM.	Major

POST Error Code	Error Message	Corrective Action	Type
854E	Memory disabled.CPU0_DIMM_E3	Remove the disabled DIMM.	Major
854F	Memory disabled.CPU0_DIMM_F1	Remove the disabled DIMM.	Major
8550	Memory disabled.CPU0_DIMM_F2	Remove the disabled DIMM.	Major
8551	Memory disabled.CPU0_DIMM_F3	Remove the disabled DIMM.	Major
8552	Memory disabled.CPU0_DIMM_G1	Remove the disabled DIMM.	Major
8553	Memory disabled.CPU0_DIMM_G2	Remove the disabled DIMM.	Major
8554	Memory disabled.CPU0_DIMM_G3	Remove the disabled DIMM.	Major
8555	Memory disabled.CPU0_DIMM_H1	Remove the disabled DIMM.	Major
8556	Memory disabled.CPU0_DIMM_H2	Remove the disabled DIMM.	Major
8557	Memory disabled.CPU0_DIMM_H3	Remove the disabled DIMM.	Major
8558	Memory disabled.CPU1_DIMM_A1	Remove the disabled DIMM.	Major
8559	Memory disabled.CPU1_DIMM_A2	Remove the disabled DIMM.	Major
855A	Memory disabled.CPU1_DIMM_A3	Remove the disabled DIMM.	Major
855B	Memory disabled.CPU1_DIMM_B1	Remove the disabled DIMM.	Major
855C	Memory disabled.CPU1_DIMM_B2	Remove the disabled DIMM.	Major
855D	Memory disabled.CPU1_DIMM_B3	Remove the disabled DIMM.	Major
855E	Memory disabled.CPU1_DIMM_C1	Remove the disabled DIMM.	Major
855F (Go to 85D0)	Memory disabled.CPU1_DIMM_C2	Remove the disabled DIMM.	Major
8560	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_A1		Major
8561	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_A2		Major
8562	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_A3		Major
8563	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_B1		Major
8564	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_B2		Major
8565	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_B3		Major
8566	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_C1		Major
8567	Memory encountered a Serial Presence Detection (SPD) failure.CPU0_DIMM_C2		Major
8568	Memory encountered a Serial Presence Detection (SPD) failure.CPU0_DIMM_C3		Major
8569	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_D1		Major
856A	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_D2		Major
856B	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_D3		Major
856C	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_E1		Major
856D	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_E2		Major
856E	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_E3		Major

POST Error Code	Error Message	Corrective Action	Type
856F	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_F1		Major
8570	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_F2		Major
8571	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_F3		Major
8572	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_G1		Major
8573	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_G2		Major
8574	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_G3		Major
8575	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_H1		Major
8576	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_H2		Major
8577	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_H3		Major
8578	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_A1		Major
8579	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_A2		Major
857A	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_A3		Major
857B	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_B1		Major
857C	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_B2		Major
857D	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_B3		Major
857E	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_C1		Major
857F (Go to 85E0)	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_C2		Major
85C0	Memory failed test/initialization CPU1_DIMM_C3	Remove the disabled DIMM.	Major
85C1	Memory failed test/initialization CPU1_DIMM_D1	Remove the disabled DIMM.	Major
85C2	Memory failed test/initialization CPU1_DIMM_D2	Remove the disabled DIMM.	Major
85C3	Memory failed test/initialization CPU1_DIMM_D3	Remove the disabled DIMM.	Major
85C4	Memory failed test/initialization CPU1_DIMM_E1	Remove the disabled DIMM.	Major
85C5	Memory failed test/initialization CPU1_DIMM_E2	Remove the disabled DIMM.	Major
85C6	Memory failed test/initialization CPU1_DIMM_E3	Remove the disabled DIMM.	Major
85C7	Memory failed test/initialization CPU1_DIMM_F1	Remove the disabled DIMM.	Major
85C8	Memory failed test/initialization CPU1_DIMM_F2	Remove the disabled DIMM.	Major
85C9	Memory failed test/initialization CPU1_DIMM_F3	Remove the disabled DIMM.	Major
85CA	Memory failed test/initialization CPU1_DIMM_G1	Remove the disabled DIMM.	Major
85CB	Memory failed test/initialization CPU1_DIMM_G2	Remove the disabled DIMM.	Major
85CC	Memory failed test/initialization CPU1_DIMM_G3	Remove the disabled DIMM.	Major
85CD	Memory failed test/initialization CPU1_DIMM_H1	Remove the disabled DIMM.	Major
85CE	Memory failed test/initialization CPU1_DIMM_H2	Remove the disabled DIMM.	Major

POST Error Code	Error Message	Corrective Action	Type
85CF	Memory failed test/initialization CPU1_DIMM_H3	Remove the disabled DIMM.	Major
85D0	Memory disabled.CPU1_DIMM_C3	Remove the disabled DIMM.	Major
85D1	Memory disabled.CPU1_DIMM_D1	Remove the disabled DIMM.	Major
85D2	Memory disabled.CPU1_DIMM_D2	Remove the disabled DIMM.	Major
85D3	Memory disabled.CPU1_DIMM_D3	Remove the disabled DIMM.	Major
85D4	Memory disabled.CPU1_DIMM_E1	Remove the disabled DIMM.	Major
85D5	Memory disabled.CPU1_DIMM_E2	Remove the disabled DIMM.	Major
85D6	Memory disabled.CPU1_DIMM_E3	Remove the disabled DIMM.	Major
85D7	Memory disabled.CPU1_DIMM_F1	Remove the disabled DIMM.	Major
85D8	Memory disabled.CPU1_DIMM_F2	Remove the disabled DIMM.	Major
85D9	Memory disabled.CPU1_DIMM_F3	Remove the disabled DIMM.	Major
85DA	Memory disabled.CPU1_DIMM_G1	Remove the disabled DIMM.	Major
85DB	Memory disabled.CPU1_DIMM_G2	Remove the disabled DIMM.	Major
85DC	Memory disabled.CPU1_DIMM_G3	Remove the disabled DIMM.	Major
85DD	Memory disabled.CPU1_DIMM_H1	Remove the disabled DIMM.	Major
85DE	Memory disabled.CPU1_DIMM_H2	Remove the disabled DIMM.	Major
85DF	Memory disabled.CPU1_DIMM_H3	Remove the disabled DIMM.	Major
85E0	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_C3		Major
85E1	Memory encountered a Serial Presence Detection (SPD) failure. CPU1_DIMM_D1		Major
85E2	Memory encountered a Serial Presence Detection (SPD) failure.CPU1_DIMM_D2		Major
85E3	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_D3		Major
85E4	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_E1		Major
85E5	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_E2		Major
85E6	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_E3		Major
85E7	Memory encountered a Serial Presence Detection (SPD) failure.CPU1_DIMM_F1		Major
85E8	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_F2		Major
85E9	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_F3		Major
85EA	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_G1		Major
85EB	Memory encountered a Serial Presence Detection (SPD) failure. CPU1_DIMM_G2		Major
85EC	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_G3		Major
85ED	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_H1		Major
85EE	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_H2		Major
85EF	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_H3		Major

POST Error Code	Error Message	Corrective Action	Type
8604	POST Reclaim of non-critical NVRAM variables		Minor
8605	BIOS settings are corrupted		Major
8606	NVRAM variable space was corrupted and has been reinitialized		Major
8607	Recovery boot has been initiated. **Note:** The Primary BIOS image may be corrupted, or the system may hang during POST. A BIOS update is required.		Fatal
A100	BIOS ACM Error		Major
A421	PCI component encountered a SERR error		Fatal
A5A0	PCI Express component encountered a PERR error		Minor
A5A1	PCI Express component encountered an SERR error		Fatal
A6A0	DXE Boot Services driver: Not enough memory available to shadow a Legacy Option ROM.	Disable option ROM at SETUP to save runtime memory.	Minor

D.1   POST Error Beep Codes

The following table lists the POST error beep codes. Before system video initialization, the BIOS uses these beep codes to inform users on error conditions. The beep code is followed by a user-visible code on the diagnostic LEDs.

Table 63. POST Error Beep Codes

Beeps	Error Message	POST Progress Code	Description
3 short	Memory error	Multiple	System halted because a fatal error related to the memory was detected.
3 long and 1 short	CPU mismatch error	E5, E6	System halted because a fatal error related to the CPU family/core/cache mismatch was detected.

The integrated BMC may generate beep codes upon detection of failure conditions. Beep codes are sounded each time that the problem is discovered, such as on each power-up attempt, but are not sounded continuously. Codes that are common across all Intel® server boards and systems that use same generation chipset are listed in the following table. Each digit in the code is represented by a sequence of beeps whose count is equal to the digit.

Table 64. Integrated BMC Beep Codes

Code	Reason for Beep	Associated Sensors
1-5-1-2	VR Watchdog Timer sensor assertion.	VR Watchdog Timer.
1-5-1-4	A PSU reports a failure, or the BMC detects the presence of a PSU model that is incompatible with one or more other PSUs in the system.	PS Status.
1-5-2-1	No CPUs installed or the first CPU socket is empty.	CPU Missing sensor.
1-5-2-2	CPU CAT Error (IERR) assertion.	CPU Status sensor.
1-5-2-3	CPU ERR2 timeout assertion.	CPU ERR2 Timeout sensor.
1-5-2-4	CPU/VR mismatch.	CPU Status sensor (configuration error offset).
1-5-2-5	CPU population error.	CPU 0 Status sensor.
1-5-4-2	Power fault: DC power is unexpectedly lost (power good dropout).	Power Unit – Power unit failure offset.
1-5-4-4	Power control fault (power good assertion timeout).	Power Unit – Soft power control failure offset.

D.2   Processor Initialization Error Summary

The following table describes mixed processor conditions and actions for all Intel® server boards and Intel® server systems designed with the Intel® Xeon® Scalable processor family architecture. The errors fall into one of the following categories:

- **Fatal**: The system halts with a halt error code on the diagnostic LEDs and a corresponding sequence consisting of three long flashes and one short flash is sent to the POST Error Code LED. The system cannot boot unless the error is resolved. The faulty component must be replaced.

- **Major**: If the BIOS Setup option "POST Error Pause" is enabled, the system goes directly to the BIOS Setup Error Manager to display the error and logs the POST error code to SEL. User intervention is required to continue booting the system. If the BIOS Setup option "POST Error Pause" is disabled, the system continues to boot and no prompt for the error is given, although the POST error code is logged to the BIOS Setup Error Manager and to the SEL.

- Minor: An error message may be displayed to the screen or to the BIOS Setup Error Manager screen and the POST error code is logged to the SEL. The system continues booting in a degraded state. The user may want to replace the erroneous unit. The POST Error Pause option setting in the BIOS setup utility does not affect this error.

Table 65. Mixed Processor Configurations Error Summary

Error	Severity	System Action when BIOS Detects the Error Condition
Processor family not identical	Fatal	• Halts with error code "0xE5" on the diagnostic LED. • Sends three long flashes and one short flash to the POST Error LED. • Does not boot until the fault condition is remediated.
Processor model not identical	Fatal	• Halts with error code "0xE5" on the diagnostic LED. • Sends three long flashes and one short flash to the POST Error LED. • Does not boot until the fault condition is remediated.
Processor cache or home agent not identical	Fatal	• Halts with error code "0xE5" on the diagnostic LED. • Sends three long flashes and one short flash to the POST Error LED. • Does not boot until the fault condition is remediated.
Processor frequency (speed) not identical	Fatal	• Halts with error code "0xE5" on the diagnostic LED. • Sends three long flashes and one short flash to the POST Error LED. • Does not boot until the fault condition is remediated.
Processor Intel® UPI link frequencies not identical	Fatal	• Halts with error code "0xE5" on the diagnostic LED. • Sends three long flashes and one short flash to the POST Error LED. • Does not boot until the fault condition is remediated.
Processor microcode update failed	Major	• Logs the POST error code "81 6x" into the SEL. • If the "POST Error Pause" is enabled in the BIOS Setup, loads the BIOS Error Manager to present error message "816x: Processor 0x unable to apply microcode update" on the screen. • If the "POST Error Pause" is disabled in the BIOS Setup continues to boot in a degraded state.

Error	Severity	System Action when BIOS Detects the Error Condition
Processor microcode update missing	Minor	• Logs the POST error code "81 8x" into the SEL. • The system continues to boot in a degraded state, regardless of the "POST Error Pause" setting in the BIOS setup. • The Error Manager in BIOS Setup will present the message "818x: Processor microcode update not found"

Appendix E. Statement of Volatility

The tables in this section are used to identify the volatile and non-volatile memory components of the Intel® Server Board M50FCP2SBSTD.

The tables provide the following data for each identified component.

- **Component Type**: Three types of components are on the server board assembly:
  - Non-volatile: Non-volatile memory is persistent and is not cleared when power is removed from the system. Non-volatile memory must be erased to clear data. The exact method of clearing these areas varies by the specific component. Some areas are required for normal operation of the server, and clearing these areas may render the server board inoperable
  - Volatile: Volatile memory is cleared automatically when power is removed from the system.
  - Battery powered RAM: Battery powered RAM is similar to volatile memory but is powered by a battery on the server board. Data in battery powered RAM is persistent until the battery is removed from the server board.
- **Size**: Size of each component in bits, kilobits (Kb), megabits (Mb), bytes, kilobytes (KB), or megabytes (MB).
- **Board Location**: Board location is the physical location of each component corresponding to information on the server board silkscreen.
- **User Data**: The flash components on the server board do not store user data from the operating system. No operating system level data is retained in any listed components after AC power is removed. The persistence of information written to each component is determined by its type as described in the table.

  Each component stores data specific to its function. Some components may contain passwords that provide access to that device's configuration or functionality. These passwords are specific to the device and are unique and unrelated to operating system passwords. The specific components that may contain password data are:

- **BIOS:** The server board BIOS provides the capability to prevent unauthorized users from configuring BIOS settings when a BIOS password is set. This password is stored in BIOS flash and is only used to set BIOS configuration access restrictions.
- **BMC:** The server board supports an Intelligent Platform Management Interface (IPMI) 2.0 conformant baseboard management controller (BMC). The BMC provides health monitoring, alerting, and remote power control capabilities for the Intel server board. The BMC does not have access to operating system level data.

  The BMC supports the capability for remote software to connect over the network for health monitoring and power control purposes. This access can be configured to require authentication by a password. If configured, the BMC maintains user passwords to control this access. These passwords are stored in the BMC flash.

The Intel® Server Board M50FCP2SBSTD includes several components that can be used to store data. A list of those components is included in the following table.

Table 66. Server Board Components

Component Type	Size	Board Location	User Data	Name
Non-Volatile	64MB	U11	No	BIOS Flash
Non-Volatile	256MB	U19	No	BMC Flash
Non-Volatile	UFM 5,888 Kb M9K Memory 1,638 Kb	U1_FPGA	No	FPGA
Volatile	8Gb	U1_BMC	No	BMC SDRAM

Appendix F.   Connectors and Headers

Table 67. Connectors and Headers

Type	Description	Manufacturer	Manufacturer Part Number	Quantity	Location
Power	SATA Power Connector, 4 Pin	Joint Tech Electronic Industrial Company, Limited	A2540WV-04P46G	1	J61
Fan	6-Pin Fan Connector, Black, 2x3 Pin	Lotes* Chia Tse Terminal Industry Company, Limited	ABA-WAF-050-Y37	6	J40, J38, J44, J42, J36, J31
Fan	8-Pin Fan Connector, Black, 2x4 Pin	Foxconn* (Hon Hai Precision Industry)	HLH2047-LF00D-4H	8	J27, J35, J37, J34, J39, J43, J33, J41
I/O	Front VGA Header, Black, 2x7 Pin	Wieson* Electronic Company, Limited	G2120C888-065H	1	J21
Fan	CPU Fan Connector, Ivory, 4 Pin	Foxconn* (Hon Hai Precision Industry)	HF2704E-M1	2	J46, J47
Storage	HSBP SMBus Connector, 5 Pin	Joint Tech Electronic Industrial Company, Limited	A2506WV-05P6T	2	J57, J28
I/O	Rear USB 2.0 Connector, Black, 4 Pin	TE Connectivity Company, Limited	1734081-1	2	J4, J5
I/O	Rear USB 3.0 Connector, Blue, 9 Pin	Molex* Limited	48405-0003	1	J3
I/O	Front Panel Header, Black, 2x12 Pin	Superior Tech Company, Limited	PHED-DS024G1ABONA-N073	1	J22
Power	PSU Connector, Black, 50 Pin	FCI-Burndy Inc. (Merge in Amphenol)	10035388-102LF	2	J24, J25
I/O	Serial A Communication Port, 8 Pin	UD Electronic Corporation	RT15-MT-0005	1	J7
Power	HSBP Power Connector, 2x6 Pin	Foxconn* (HON HAI Precision Industry)	HM3506E-HP1	1	J53
Power	Power Connector, 2x2 Pin	TE Connectivity Company, Limited	4-1775099-0	5	J60, J12, J62, J51, J52
Power	Battery holder, Black, 2 Pin	Lotes* Chia Tse Terminal Industry Company, Limited	AAA-BAT-029-P02	1	BAT1
I/O	SAS module Connector, 10 Pin	Molex* Limited	53398-1071	1	J56
I/O	VGA Connector, Black, 15 Pin	Molex* Limited	47272-0001	1	J17
Firmware	TPM Connector, Black, 2x6 Pin	FCI-Burndy Inc. (Merge in Amphenol)	20021221-00312C4LF	1	J16
I/O	IDV Connector, Black, 2x20 Pin	Samtec* Incorporated	TFM-120-02-L-D-P-TR	1	J50
I/O	Front Panel Zero Insertion Force (ZIF) Connector, Gray, 26 Pin	Hirose HRS Company, Limited	FH52-26S-0.5SH	2	J55, J6
Storage	M.2 Connector, Black, 67 Pin	Bellwether Electronic Corporation	80159-8524	2	M2_CN1, M2_CN2
PCI	OCPv3 Connector, Black, 168 Pin	Amphenol* Limited	ME1016813401311	1	OCP_CN1_OCP3
PCI	Riser1/Riser2 Slot Connector, Black, 280 Pin	TE Connectivity Company, Limited	1-2328461-1	2	J1, J2
PCI	Interposer Slot Connector, Black, 56 Pin	Amphenol* Limited	ME1005610101011	1	J58
PCI	Riser3 Slot Connector, Black, 168 Pin	Amphenol* Limited	ME1016810101011	1	J32

Type	Description	Manufacturer	Manufacturer Part Number	Quantity	Location
Storage	MCIO Connector, Black, 38 Pin	Amphenol* Limited	G97V21332HR	16	J75, J74, J72, J73, J8, J69, J71, J76, J66, J70, J67, J64, J68, J30, J65, J63
Storage	Mini-SAS HD Connector, Black, 2x36 Pin	FCI-Burndy Incorporated (Merge in Amphenol)	10127912-1201LF	1	MINI_SAS_HD1
Memory	DIMM Socket, Blue, 288 Pin	Lotes* Chia Tse Terminal Industry Company, Limited	ADR50001-P023C01	16	J4_CPU0, J6_CPU1, J2_CPU1, J16_CPU0, J14_CPU1, J6_CPU0, J4_CPU1, J14_CPU0, J10_CPU0, J8_CPU1, J12_CPU1, J16_CPU1, J8_CPU0, J10_CPU1, J2_CPU0, J12_CPU0
Memory	DIMM Socket, Black, 288 Pin,	Lotes* Chia Tse Terminal Industry Company, Limited	ADR50001-P014C01	16	J9_CPU0, J9_CPU1, J7_CPU1, J1_CPU1, J11_CPU0, J1_CPU0, J5_CPU1, J11_CPU1, J5_CPU0, J3_CPU0, J7_CPU0, J13_CPU0, J3_CPU1, J15_CPU1, J15_CPU0, J13_CPU1
Firmware	BIOS Flash Socket, Black, 8 Pin	Lotes* Chia Tse Terminal Industry Company, Limited	ACA-SPI-006-K01	1	U11

Appendix G. Sensors

The following figure provides the location of the sensors on the Intel® Server Board M50FCP2SBSTD.

Note: The numbers in the following figure are hexadecimal numbers.
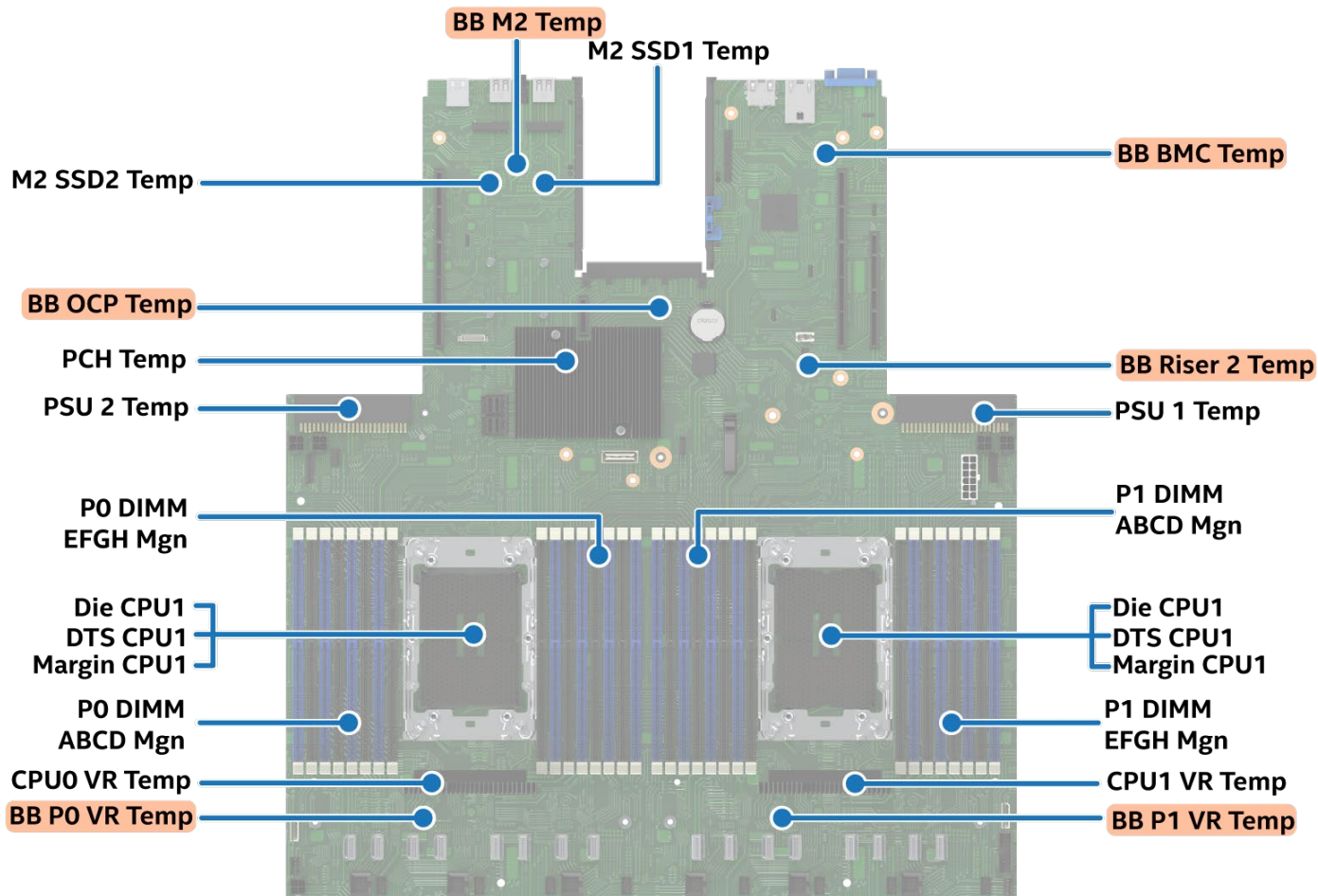
Figure 74. Server Board Sensor Map

Appendix H. Server Board Installation and Component Replacement

This appendix provides general information necessary to install the server board into a server chassis. The system integrator should reference and follow all available system assembly instructions provided by the chassis manufacturer for full system assembly instructions.

This appendix also provides instructions for processor and memory replacement. Replacement instructions for all other system options should be provided by the chassis or system manufacturer.

Safety Warnings

Heed safety instructions: Before working with your server product, whether you are using this guide or any other resource as a reference, pay close attention to the safety instructions. You must adhere to the assembly instructions in this guide to ensure and maintain compliance with existing product certifications and approvals. Use only the described, regulated components specified in this guide. Use of other products/components voids the UL listing and other regulatory approvals of the product and will most likely result in noncompliance with product regulations in one or more regions in which the product is sold.

System power on/off: The power button DOES NOT turn off the system AC power. To remove power from the system, you must unplug the AC power cord. Make sure that the AC power cord is unplugged before you open the chassis, add, or remove any components.

Hazardous conditions, devices, and cables: Hazardous electrical conditions may be present on power, telephone, and communication cables. Turn off the server and disconnect the power cord, telecommunications systems, networks, and modems attached to the server before opening it. Otherwise, personal injury or equipment damage can result.

Installing or removing jumpers: A jumper is a small plastic encased conductor that slips over two jumper pins. Some jumpers have a small tab on top that you can grip with your fingertips or with a pair of fine needle nosed pliers. If your jumpers do not have such a tab, take care when using needle nosed pliers to remove or install a jumper; grip the narrow sides of the jumper with the pliers, never the wide sides. Gripping the wide sides can damage the contacts inside the jumper, causing intermittent problems with the function controlled by that jumper. Take care to grip with, but not squeeze, the pliers or other tool you use to remove a jumper, or you may bend or break the pins on the board.

Electrostatic Discharge (ESD)

Electrostatic discharge can damage the computer or the components within it. ESD can occur without the user feeling a shock while working inside the system chassis or while improperly handling electronic devices like processors, memory or other storage devices, and add-in cards.

Intel® recommends that the following steps be taken when performing any procedures described within this document or while performing service to any computer system.

- Where available, all system integration and/or service should be performed at a properly equipped ESD workstation
- Wear ESD protective gear like a grounded antistatic wrist strap, sole grounders, and/or conductive shoes
- Wear an anti-static smock or gown to cover any clothing that may generate an electrostatic charge
- Remove all jewelry
- Disconnect all power cables and cords attached to the server before performing any integration or service
- Touch any unpainted metal surface of the chassis before performing any integration or service
- Hold all circuit boards and other electronic components by their edges only
- After removing electronic devices from the system or from their protective packaging, place them component side up on to a grounded anti-static surface or conductive workbench pad. Do not place electronic devices on to the outside of any protective packaging.

H.1   Server Board Installation Guidelines

This section provides general guidelines and recommendations for installing the server board into a server chassis. However, Intel highly recommends that system integrators follow all installation guidelines and instructions provided by the chassis manufacturer when integrating the server board into the chosen chassis.
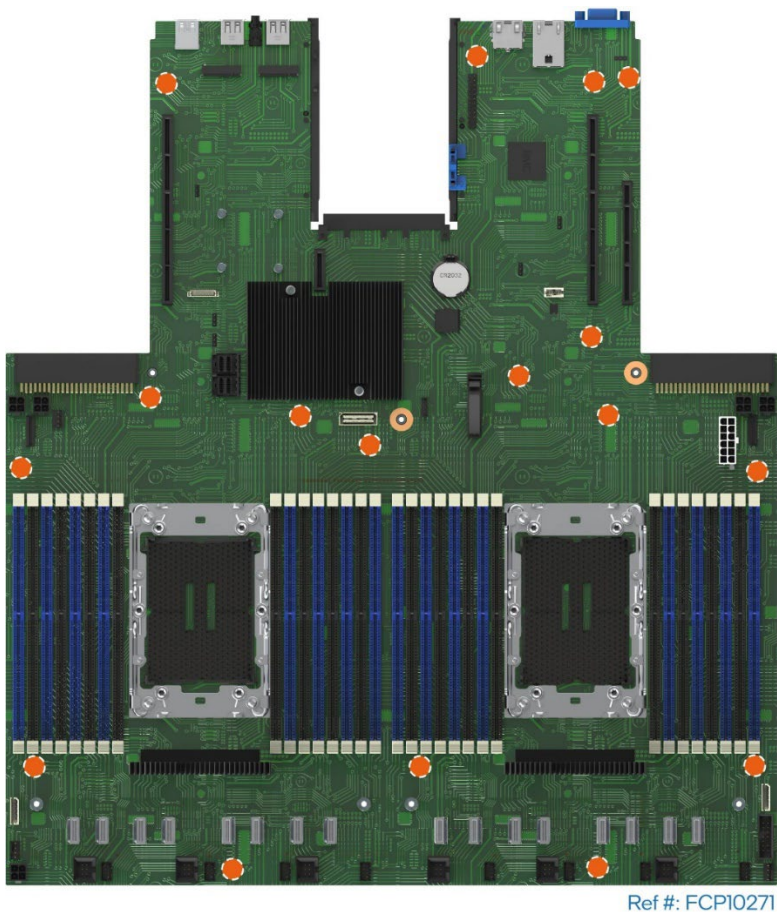

Figure 75. Server Board Mounting Hole Locations

Server chassis may use different methods for securing the server board to the chassis. The selected chassis may have integrated mounting features, or they may include separate mounting stand-offs that must be installed.

The following illustration identifies possible mounting options that can be used.
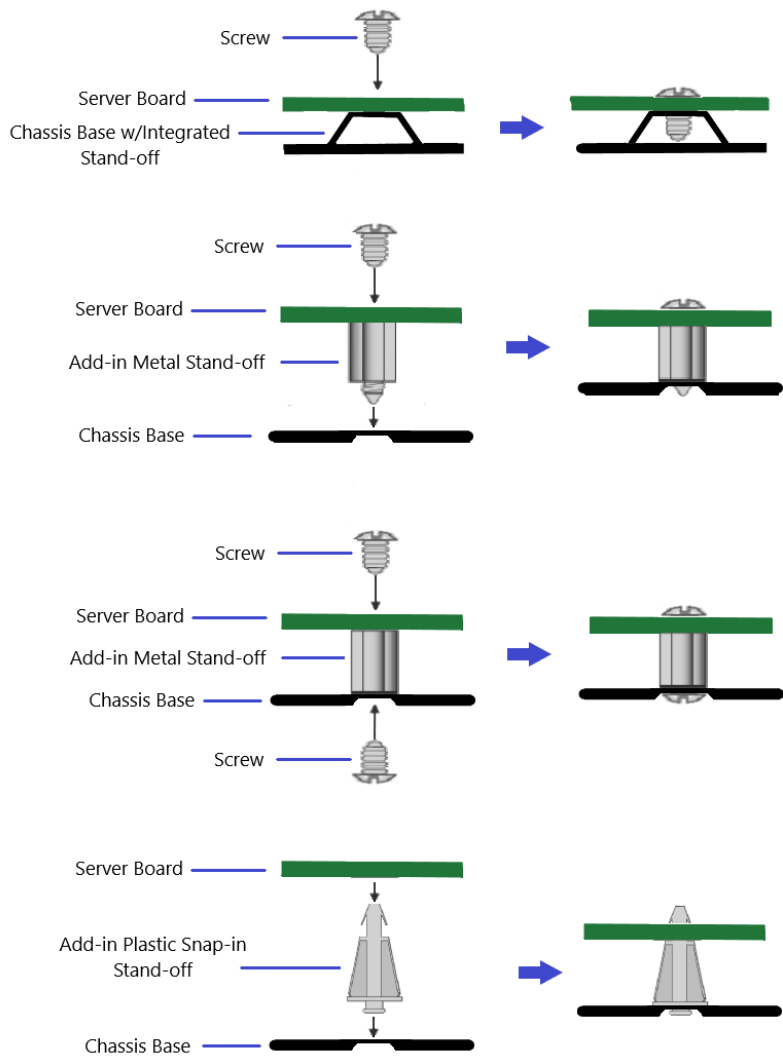
Figure 76. Possible Server Board Mounting Options

For mounting options that require the server board to be secured to the chassis using screws, Intel recommends tightening the screws using a torque or pneumatic screwdriver. The recommended torque setting is dependent on the screw type used. See the following table.

Table 68. Server Board Mounting Screw Torque Requirements

Screw Size	Torque Value	Tolerance ±
6–32	8 in-lb	1
M3	5 in-lb	1

H.2 Processor Replacement Instructions

Processors are part of an assembly referred to as a PHM (Processor Heat sink Module). A PHM consists of a processor, a processor carrier clip, and the processor heat sink that is preassembled into a single module before placement onto the processor socket assembly on the server board. The PHM concept reduces the risk of damaging pins within the processor socket during the replacement process.

The system may use 1U (Low-profile) or 2U size processor heat sinks. The following procedures can be applied to either option.

Note: The following procedure applies to processor heat sinks that are used in Intel server systems. If the processor heat sink is different from those shown in the following procedures, then Intel recommends following the processor replacement procedures included within documentation supplied with the chosen non-Intel server system.

Components Required

- New matching 4th Gen Intel® Xeon® processor Scalable processor + included shipping tray
- Existing processor carrier clip
- New processor heat sink or existing processor heat sink + new thermal interface material (TIM)

Required Tools and Supplies

- Anti-static wrist strap, an ESD safe workbench, and other anti-ESD precautions (recommended)
- ESD Gloves (recommended)
- T-30 Torx* screwdriver

Average Time to Complete ~10+ minutes

Procedure Prerequisites

- The system must be powered off and AC Power cord(s) disconnected.

Caution: Fin edges of the processor heat sink are very sharp. Intel® recommends wearing thin ESD protective gloves when handling the PHM during the following procedures.

Caution: Processor heat sinks are easily damaged if handled improperly. See the following image for proper handling.

HEAT SINK
TOP VIEW

DAMAGE CAUTION
TO PREVENT STRUCTURAL DAMAGE
HOLD THE HEAT SINK AS SHOWN.
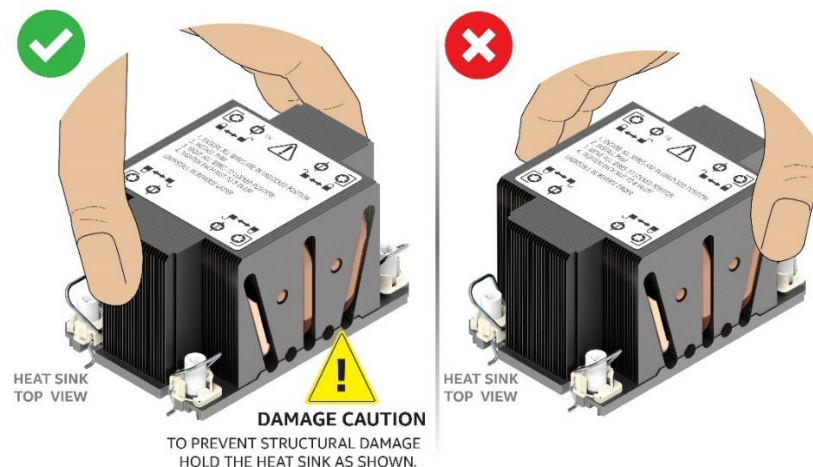
HEAT SINK
TOP VIEW

Ref #: FCP40320

Figure 77. Processor Heat Sink Handling

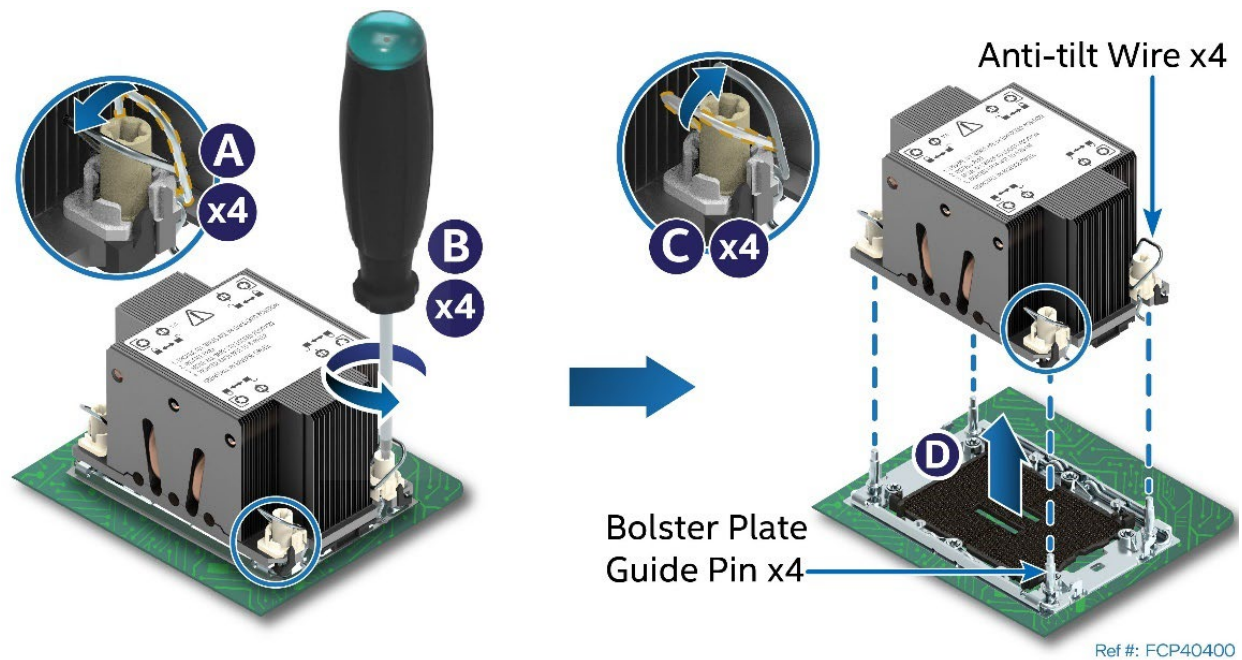# H.2.1 Processor Heat Sink Module (PHM) Removal from Server Board

Figure 78. PHM Assembly Removal from Processor Socket

1. Power off the system and disconnect the power cable(s).
2. Remove system access panel.
3. Remove or set aside all system components preventing access to the processors.
4. Ensure the anti-tilt wire on the four corners of the heat sink are in the outward position (see Letter A).
5. Fully unscrew all four heat sink fasteners in any order (see Letter B).
6. Push the anti-tilt wire on all four corners of the heatsink to the inward position (see Letter C).
7. Lift the PHM straight up and away from the server board (see Letter D).
8. Place the PHM, bottom side up, on a flat surface.
9. Visually inspect that the socket is free of damage or contamination.

Caution: If debris is observed, blow it away gently with an air blower. Do not use tweezers or any other hard tools to remove it manually.

If reinstalling the processor later, then Intel highly recommends reinstalling the processor socket protective cover that shipped with the system to prevent possible pin damage while the socket is not populated.
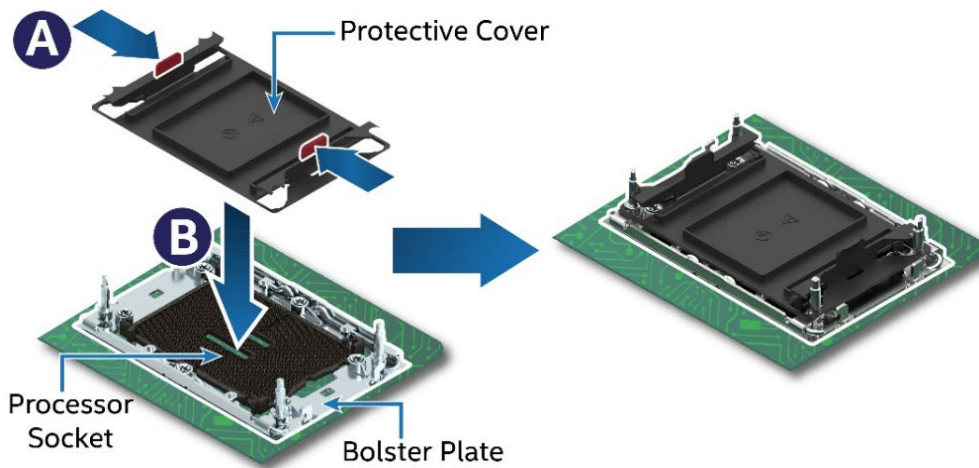
Figure 79. Reinstall the Socket Cover

- Squeeze the finger grips at each end of the cover (see Letter A in above figure) and carefully lower the cover on the socket (see Letter B), then release finger grips.
- Ensure that socket cover is locked in place.

Caution: Do not press the center of the socket cover.
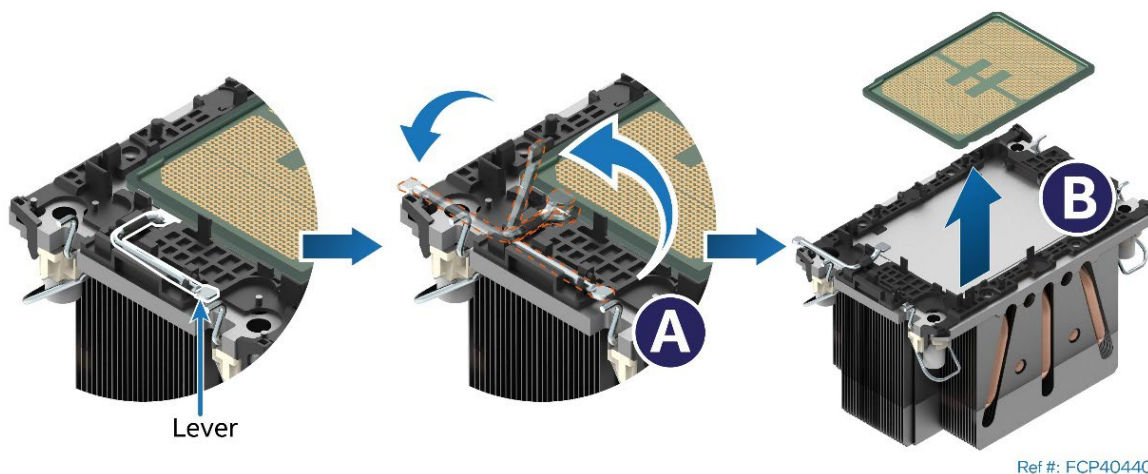
H.2.2 Processor Heat Sink Module (PHM) Disassembly

Figure 80. Processor Removal from PHM Assembly

1. While holding down the PHM, carefully rotate the lever (see Letter A) from left to right until the processor lifts from the processor carrier clip.
2. While holding down the processor carrier clip, carefully lift the processor from it (see Letter B).
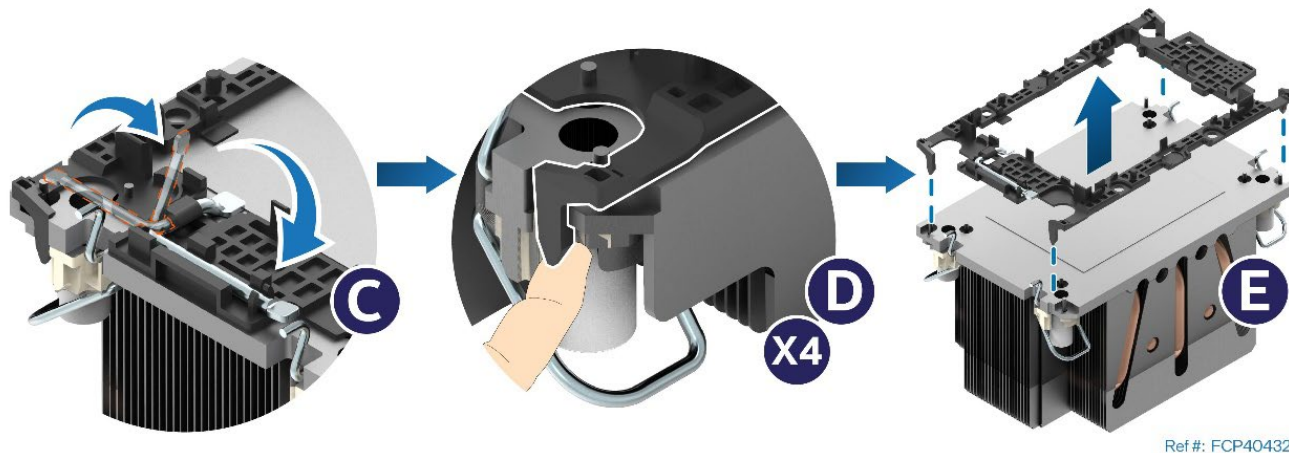
Figure 81. Processor Carrier Clip Removal from PHM Assembly

3. Return the lever to the original position (see Letter C).

4. Unlatch the tab on each corner of the processor carrier clip to release it from the heat sink (see Letter D)

5. Lift the processor carrier clip up and away from the heat sink (see Letter E).

H.2.3   Processor Heat Sink Module (PHM) Assembly

To properly assemble the PHM and install it to the server board, the procedures described in the following sections must be followed in the order specified. These instructions assume that the Thermal Interface Material (TIM) is already applied to the bottom of the heat sink.
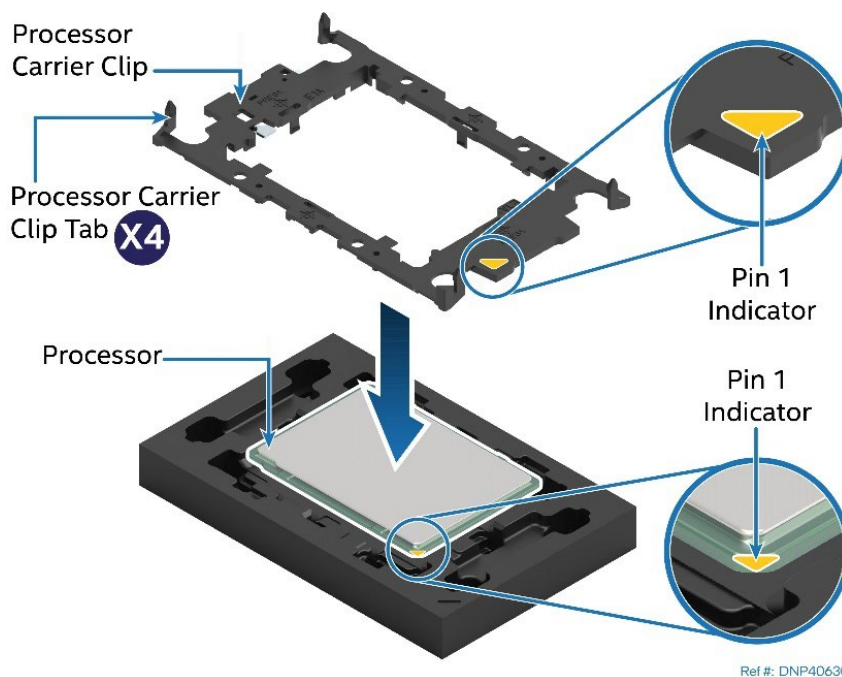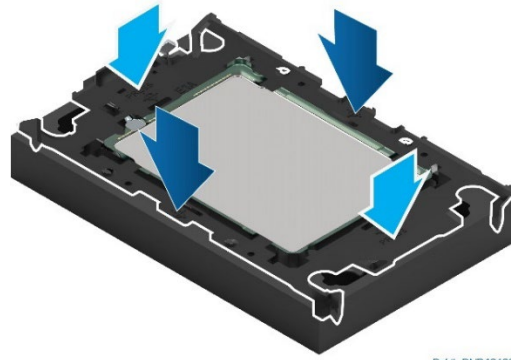

**Figure 82. Installing Processor Carrier Clip onto Processor – Part 1**

1. Orient the Pin 1 indicator of the carrier clip with the Pin 1 indicator of the processor (See Figure 82).

2. With the processor still on its shipping tray, place the processor carrier clip over the processor.

Figure 83. Installing Processor Carrier Clip onto Processor – Part 2

3. Gently press down on two opposite sides of the carrier clip until it clicks into place and repeat with the other two sides (See Figure 83).
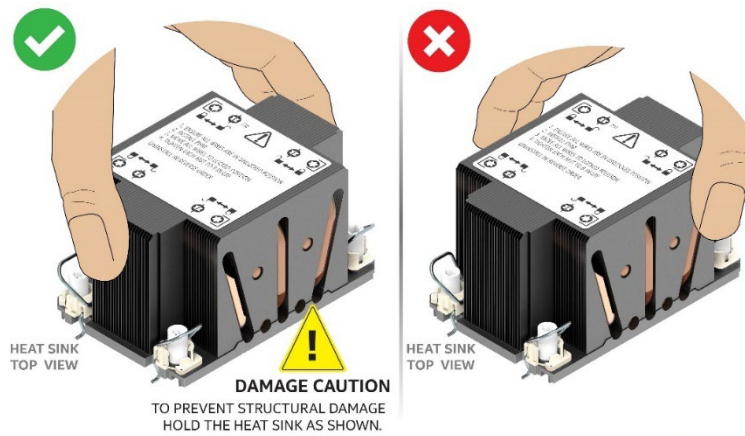
Figure 84. Removing Heat Sink from its Packaging

4. Locate the processor heat sink. To avoid damage to the heat sink, grasp it by its narrower top and bottom edges as shown in Figure 84.

Figure 85. Processor Heat Sink Anti-tilt Wires in the Outward Position

5. Set the anti-tilt wire on all four corners of the heat to their outward position.
6. Turn the heat sink over and place it bottom side up on a flat surface.

7. Clean any residual old Thermal Interface Material (TIM) from the heat sink and apply new TIM.
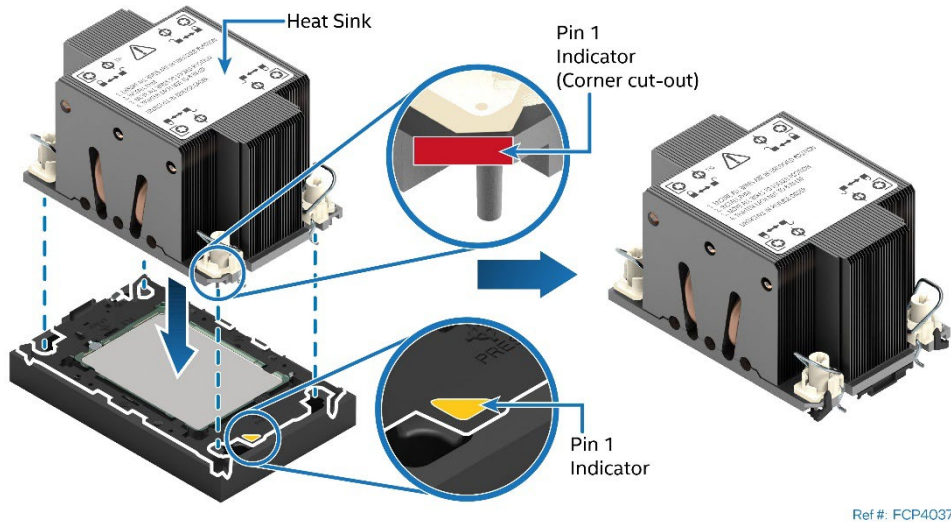

Figure 86. Pin 1 Indicator of Processor Carrier Clip

8. Carefully lift and turn over the heat sink.

9. Align the Pin 1 indicator of the processor carrier clip with the corner cut-out on the heat sink (See Figure 86)

Note: For the standard 2U or 1U heat sink, there are two cut-out corners; either can be used to align Pin 1 indicators.

10. Gently press the heat sink down onto the processor carrier clip until it clicks into place.

11. Ensure that all four heat sink corners are securely latched to the carrier clip tabs.

H.2.4 Processor Heat Sink Module (PHM) Installation to Server Board

Caution: Do not touch the processor socket pins. The pins inside the processor socket are extremely sensitive. A damaged processor socket may produce unpredictable system errors.
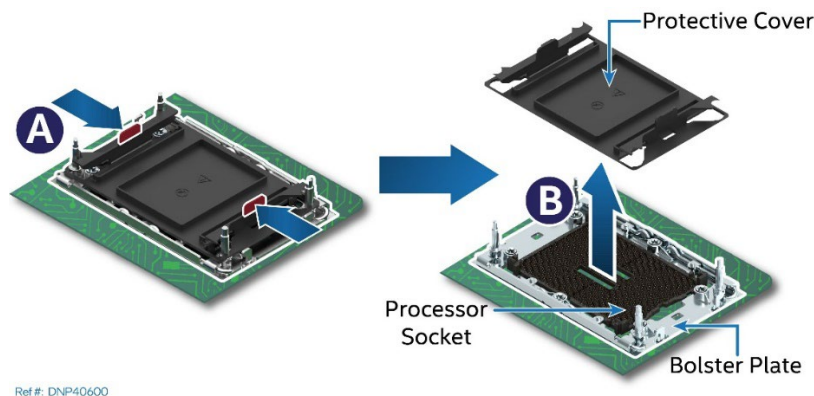

Figure 87. Socket Protective Cover Removal

1. (If present) Remove the processor socket cover by squeezing the finger grips (see Letter A) and pulling the cover up and away from the processor socket (see Letter B).

Caution: Ensure that the processor socket is free of damage or contamination before installing the PHM. If debris is observed, blow it away gently with an air blower. Do not use tweezers or any other hard tools to remove it manually.
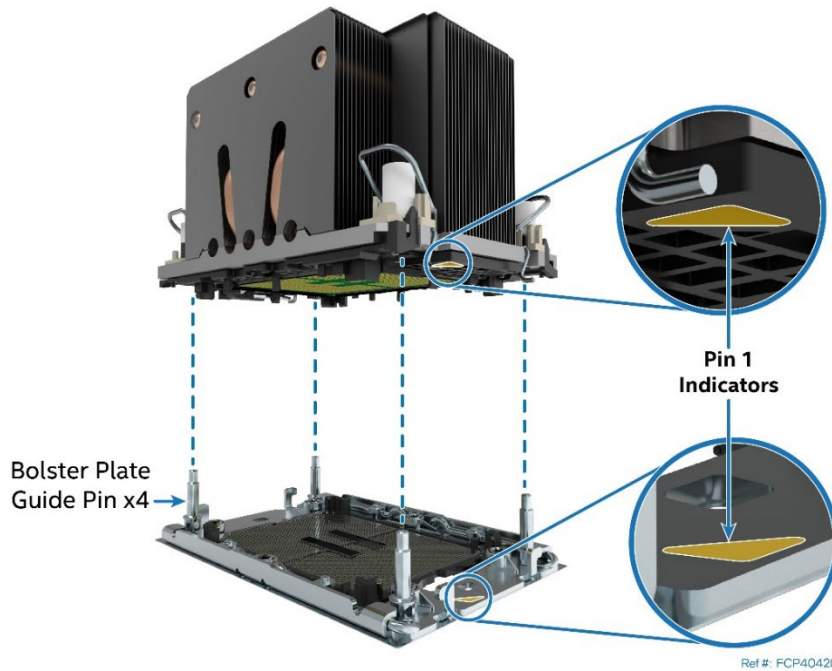

Figure 88. PHM Alignment with Socket Assembly

2. Set anti-tilt wires on all four corners of the heat sink to the inward position (see Letter A in Figure 89).

3. Align the Pin 1 indicators of the processor carrier clip and processor with the Pin 1 indicator on the bolster plate located around the processor socket (See Figure 88).

Caution: Processor socket pins are delicate and bend easily. Use extreme care when placing the PHM onto the processor socket. Do not drop it.
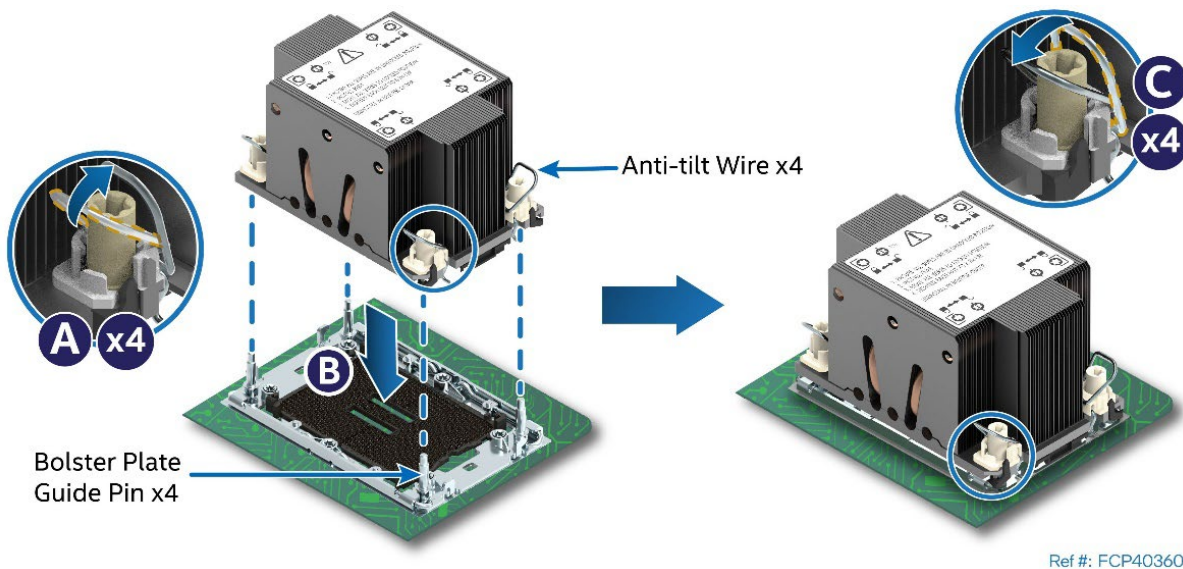

Figure 89. PHM Installation onto Server Board

4. Carefully lower the PHM onto the bolster plate alignment pins (see Letter B).

5. Set all four anti-tilt wires on the heat sink to the outward position (see Letter C).
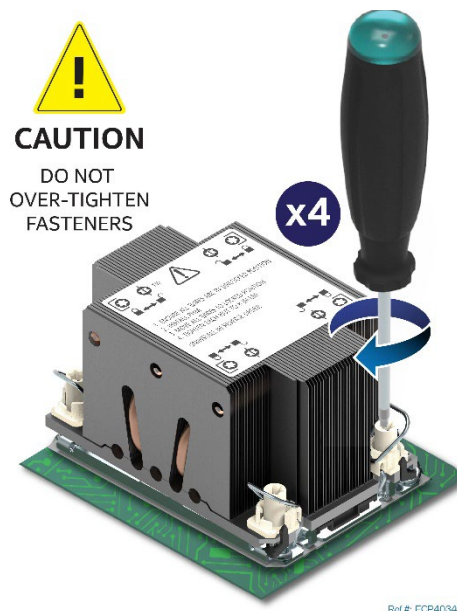
Figure 90. Tighten Heat Sink Fasteners

6. Tighten the heat sink fasteners using a T30 Torx* screwdriver to 8 in-lb. No specific sequence is needed for tightening.

Important: A processor socket cover should be installed onto any unpopulated processor socket. Do not install a processor heat sink over a processor socket that is empty.

H.3   DIMM / Intel® Optane™ PMem Replacement Instructions

Required Tools and Supplies

- Anti-static wrist strap and conductive workbench pad (recommended)
- Replacement equivalent memory module

Average Time to Complete: ~ 5 minutes (Complete Intel® Optane™ PMem replacement and setup is longer).

Procedure Prerequisites

- Memory modules are NOT hot-swappable. The system must be powered down and unplugged from the AC power source before replacing a faulty memory module in the system.

Instructions to physically replace a DDR5 DIMM or an Intel® Optane™ PMem 300 series module are the same. For the following procedure, Standard DDR5 DIMMs and Intel® Optane™ PMem devices are commonly referred to as "memory module".
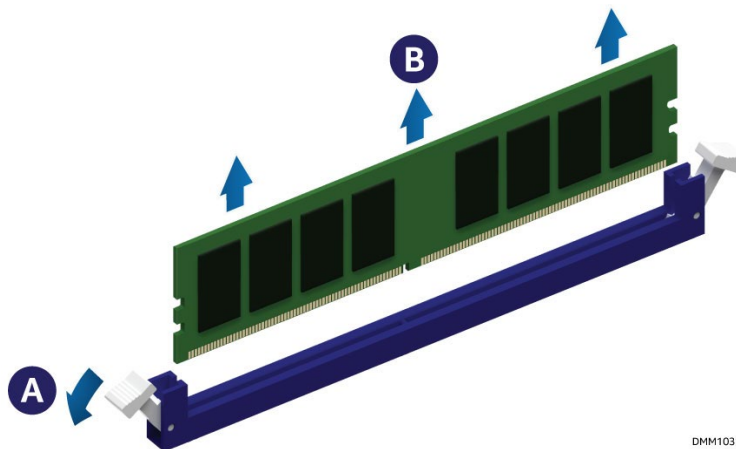
DMM1031

Figure 91. Memory Module Removal

1. Identify and locate the faulty memory module.
2. Ensure that the ejection tabs of adjacent memory slots are fully closed.
3. Open the ejection tabs at both ends of the selected memory slot (see Letter A). The memory module lifts slightly out from the memory slot.
4. Holding the memory module by its edges, lift it away from the slot (see Letter B in Figure 91).

BNP053
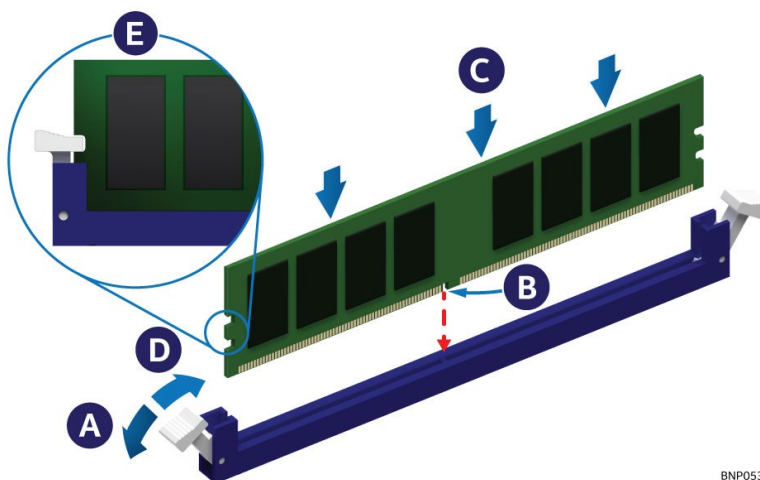
Figure 92. DIMM Installation

5. Ensure that the ejection tabs at both ends of the memory slot are pushed outward to the open position (see Letter A).
6. Carefully unpack the replacement memory module, taking care to only handle the device by its outer edges.
7. Align the notch at the bottom edge of the memory module with the key in the memory slot (see Letter B).
8. Insert the memory module into the memory slot.
    *   Using even pressure along the top edge, push down on the memory module (see Letter C) until the ejection tabs of the memory slot snap into place (see Letter D).
9. Ensure that the ejection tabs are firmly in place (see Letter E).

Note: Replacing Intel® Optane™ PMem devices requires additional steps to enable and configure them. Refer to the appropriate Intel® Optane™ PMem documentation to complete the installation process for these devices.

Appendix I.   Supported Intel® Server Systems

The Intel® Server Board M50FCP2SB is designed to be integrated into high density 1U and 2U rack mount server chassis. Intel® server systems in this server board family include the 2U Intel® Server System M50FCP2UR and the 1U Intel® Server Systems M50FCP1UR. The sections below provide a high-level overview of the features associated with each. For additional product information, refer to the Technical Product Specification, Integration and Service Guide, Product Family Configuration Guide, and other marketing material available for each of these Intel server products.

I.1   Intel® Server System M50CYP2UR Family
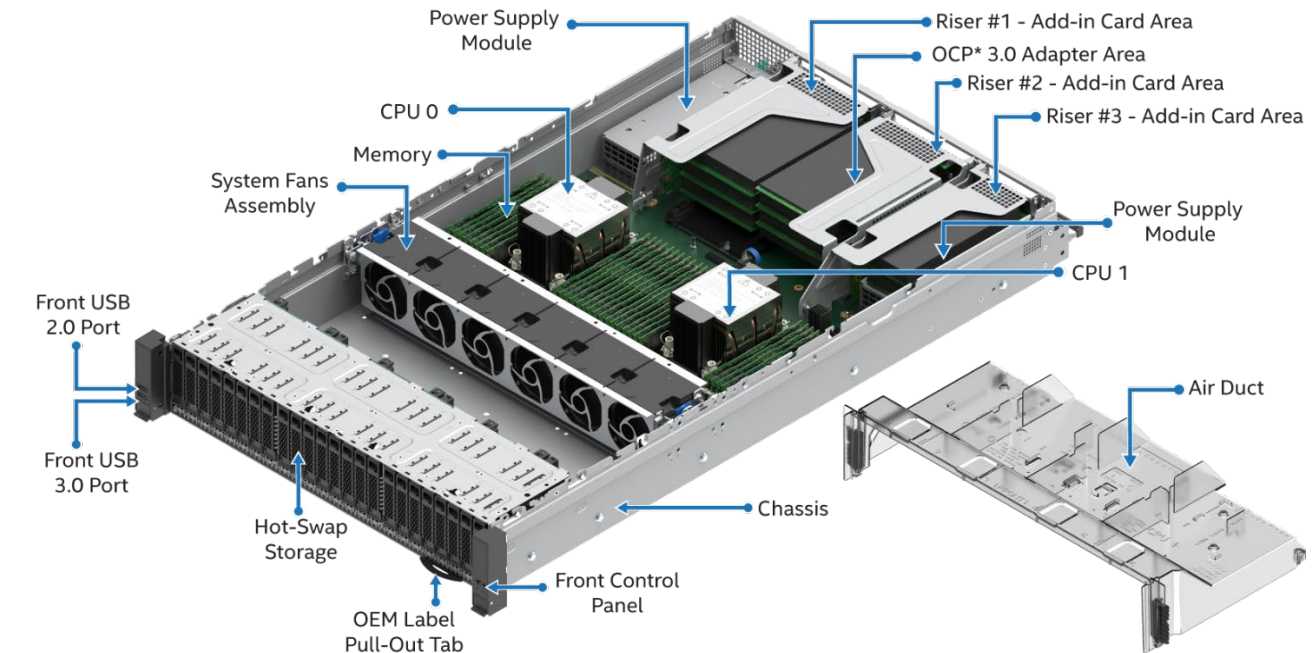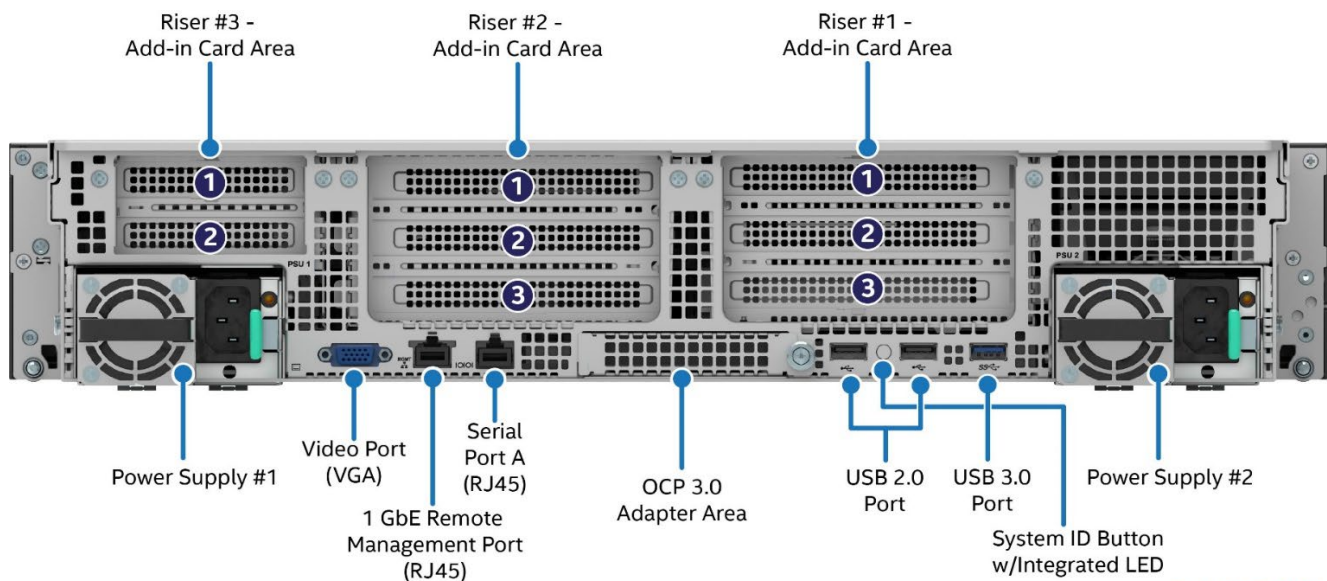
Figure 93. Intel® Server System M50FCP2UR Family

Table 69. Intel® Server System M50FCP2UR Family Features

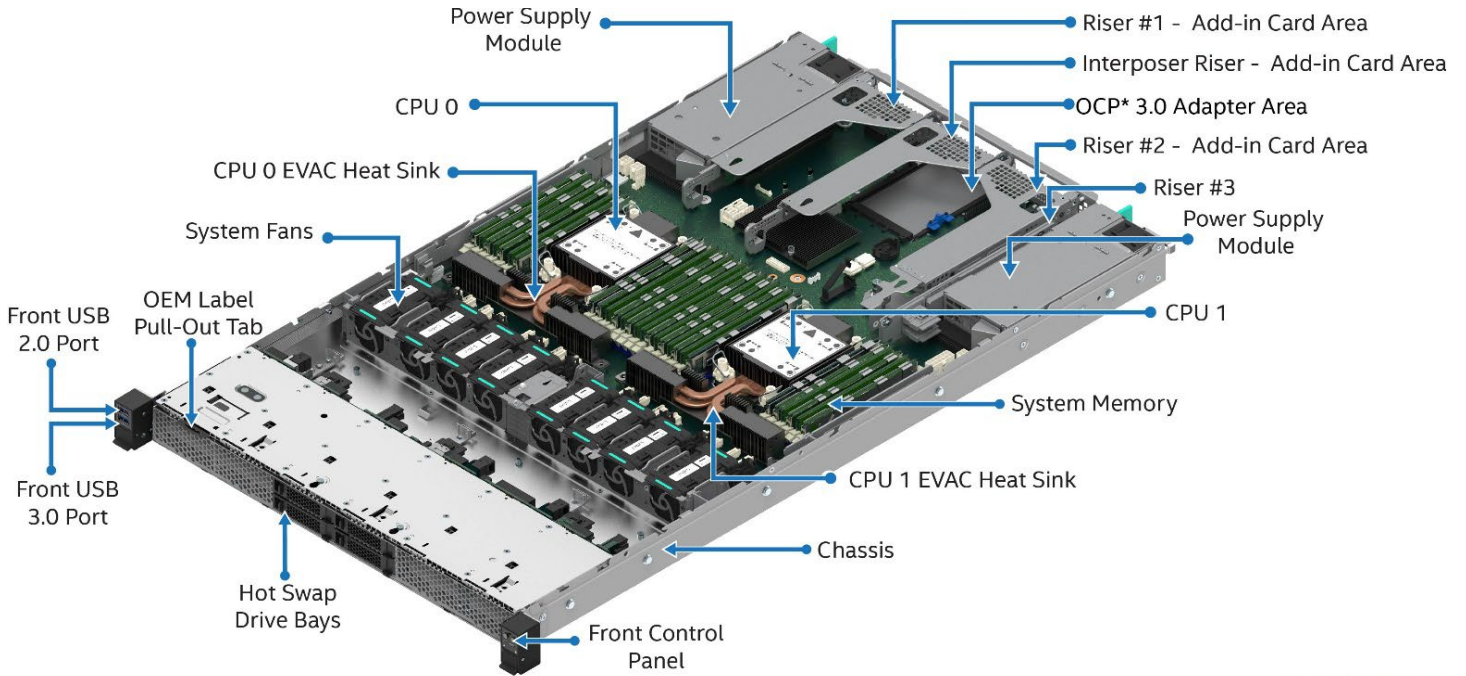| Feature	Details
Chassis Type	2U rack mount chassis
Chassis Dimensions	769.6 x 438 x 87 mm (L x W x H)
Server Board	Intel® Server Board M50FCP2SBSTD

Processor Support	• Dual Socket- E LGA4677
	• Supported 4th Gen Intel® Xeon® Scalable processor family SKUs:
	  o Intel® Xeon® Platinum 84xxxx processor
	  o Intel® Xeon® Gold 64xxxx processor
	  o Intel® Xeon® Gold 54xxxx processor
	  o Intel® Xeon® Silver 44xxxx processor
	  o Intel® Xeon® Bronze 34xxxx processor
	• Intel® UPI links: up to 3 at 16 GT/s (Platinum and Gold) or up to 2 at 16 GT/s (Silver)
	• Intel® Xeon® Bronze processors are used in single processor configurations only.
	
	Notes:
	Previous generation Intel® Xeon® processor and Intel® Xeon® Scalable processor families are not supported.
	For processor support details, see the Intel® Server Board M50FCP2SBSTD Technical Product Specification.

Maximum Supported Processor Thermal Design Power (TDP)	• Up to 350 W. **Note:** The maximum supported processor TDP is dependent on the system configuration. See product TPS for additional information

Chipset	• Intel® C741 chipset platform controller hub (PCH)
	• Embedded features enabled on this server board:
	  o SATA 3.0 support
	  o USB 3.0 support
	  o PCIe 3.0 support

Memory Support	• 32 memory slots
	  o 16 memory slots per processor, eight memory channels per processor
	  o Two memory modules per channel
	• Registered DDR5 DIMM (standard RDIMM, 3DS-RDIMM, and 9x4 RDIMM)
	  Note: 3DS = 3-dimensional stacking.
	• All DDR5 DIMMs must support ECC
	• Intel® Optane™ PMem 300 series (App Direct Mode support only)
	• Memory capacity
	  o Up to 12 TB per processor (processor SKU dependent) using DDR5 DIMMs combined with Intel Optane PMem 300 series modules
	• Memory data transfer rates
	  o Up to 4800 MT/s at one DIMM per channel (processor SKU dependent)
	  o Up to 4400 MT/s at two DIMMs per channel (processor SKU dependent)
	• DDR5 standard voltage of 1.1 V
	
	Note: For memory support details, see the *Intel® Server Board M50FCP2SBSTD Technical Product Specification*.

System Fan Support	• Six managed 60-mm hot swap capable system fans • Integrated fans included with each installed power supply module

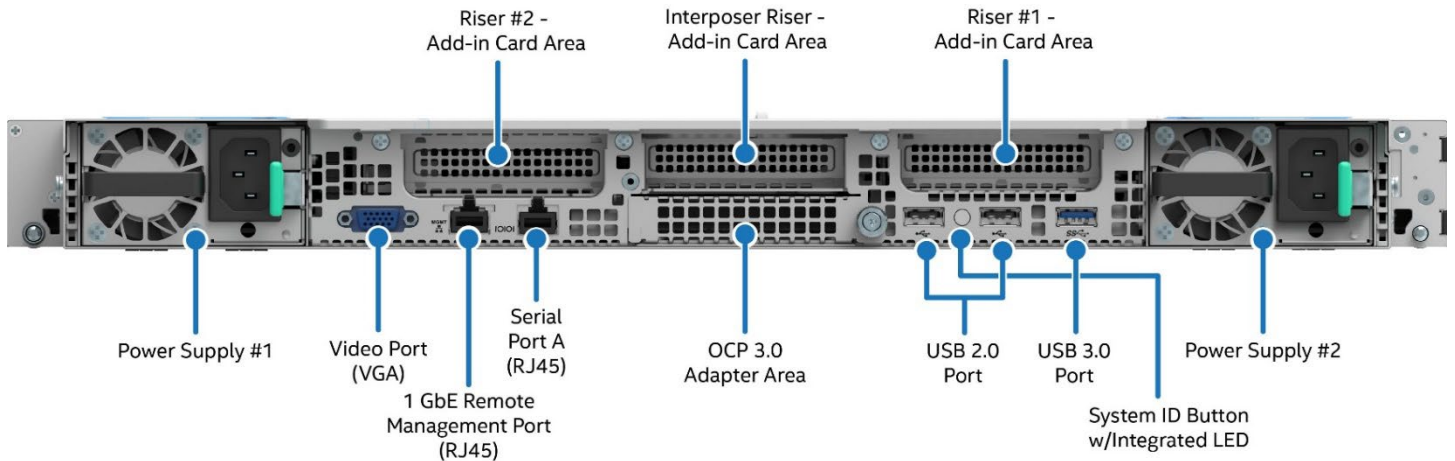| Feature	Details
Power Supply Options	- The server system can support one or two power supply modules configurations. - Depending on the power supply configuration, the system will support the following power operating modes: 1+0 – Single functional power supply 1+1 – redundant power 2+0 – combined power, no redundancy - Power supply options: - AC 1300 W Titanium - AC 1600 W Titanium - AC 2100 W Platinum
Onboard Network Support	Provided by optional Open Compute Project* (OCP*) adapter support.
Open Compute Project* (OCP*) Adapter Support	Server board x16 PCIe 5.0 OCP 3.0 connector (Small Form-Factor) slot. Refer to https://servertools.intel.com/sct for the latest list of adapters supported by the server board.
Riser Card Support	Concurrent support for up to three riser cards with support for up to eight PCIe add-in cards. In the following description FH = Full Height, FL = Full Length, HL =Half Length, LP = Low Profile. **Riser Slot #1** - Riser Slot #1 supports x32 PCIe lanes, routed from CPU 0 - PCIe 5.0 support for up to 64 GB/s **Riser Slot #1 supports the following Intel riser card options:** - Two PCIe slot riser card (iPC **FCP2URISER1DW**), which support: - One FH/FL double-width slot (x16 electrical, x16 mechanical) - One FH/HL single-width slot (x16 electrical, x16 mechanical) - Two PCIe slot riser card (iPC **FCP2URISER1SW**), which support: - Two FH/FL single-width slot (x16 electrical, x16 mechanical) - Three PCIe slot riser card (iPC **FCP2URISER1STD**), which support: - One FH/FL single-width slot (x16 electrical, x16 mechanical) - One FH/FL single-width slot (x8 electrical, x16 mechanical) - One FH/HL single-width slot (x8 electrical, x8 mechanical) - NVMe riser card (iPC **FCP2URISER1RTM**), which supports: - One HL or FL single-width slot (x16 electrical, x16 mechanical) - Two x8 PCIe NVMe MCIO connectors, each with a re-timer **Riser Slot #2** - Riser Slot #2 supports x32 PCIe lanes, routed from CPU 1 - PCIe 5.0 support for up to 64 GB/s **Riser Slot #2 supports the following Intel riser card options:** - Two PCIe slot riser card (iPC **FCP2URISER2DW**), which support: - One FH/FL double-width slot (x16 electrical, x16 mechanical) - One FH/HL single-width slot (x16 electrical, x16 mechanical) - Two PCIe slot riser card (iPC **FCP2URISER2SW**), which support: - Two FH/FL single-width slot (x16 electrical, x16 mechanical) - Three PCIe slot riser card (iPC **FCP2URISER2STD**), which support: - One FH/FL single-width slot (x16 electrical, x16 mechanical) - One FH/FL single-width slot (x8 electrical, x16 mechanical) - One FH/HL single-width slot (x8 electrical, x8 mechanical)

Feature	Details

Risser Card Support (Cont.)	**Riser Slot #3**
	• Riser Slot #3 supports x16 PCIe lanes, routed from CPU 1
	• PCIe 5.0 support for up to 32 GB/s
	Riser Slot #3 supports the following Intel riser card options:
	• Two PCIe slot riser card (iPC **FCP2URISER3STD**), which support:
	  o Two LP/HL single-width slots (x16 mechanical, x8 electrical)
	• NVMe riser card (iPC **CYPRISER3RTM**), which supports:
	  o Two PCIe NVMe SlimSAS connectors with re-timers

PCIe* NVMe* Support	• Supports up to 18 PCIe NVMe interconnects
	  o 16 server board MCIO connectors, eight per processor
	  o Two M.2 NVMe/SATA connectors
	• Additional NVMe support through select Riser Card options (see Riser Card Support)
	• Volume Management Device (VMD) support

Video Support	• Integrated 2D video controller • 128 MB of DDR4 video memory • One VGA connector on the rear of the chassis

Onboard SATA Support	• 10 x SATA III ports (6 Gb/s, 3 Gb/s, and 1.5 Gb/s transfer rates supported)
	  o Two M.2 connectors: SATA/PCIe
	  o Two 4-port Mini-SAS HD (SFF-8643) connectors

USB Support	• One USB 3.0 and two USB 2.0 connectors on the rear of the chassis • One USB 3.0 and one USB 2.0 connector on the front panel
Serial Support	• One external RJ-45 Serial Port A connector on the rear of the chassis
Front Drive Bay Options	• 8 x 2.5" SAS/SATA/NVMe hot swap drive bays – iPC M50FCP2UR208 • 16 x 2.5" SAS/SATA/NVMe hot swap drive bays - iPC M50FCP2UR208 with installed accessory kits • 24 x 2.5" SAS/SATA/NVMe hot swap drive bays - iPC M50FCP2UR208 with installed accessory kits • 12 x 3.5" SAS/SATA hot swap drive bays (supports up to 4 NVMe drives) - iPC M50FCP2UR312
Server Management	• Integrated Baseboard Management Controller (BMC) • One dedicated RJ45 1 GbE server management port • Intelligent Platform Management Interface (IPMI) 2.0 compliant • Redfish* compliant • Support for Intel® Data Center Manager (Intel® DCM) • Support for Intel® Server Debug and Provisioning Tool (Intel® SDP Tool) • Support for Intel® Server Management Software • Intel® Light-Guided Diagnostics • Optional Advanced Server Management features (Purchased separately)

Server Management Processor (SMP)	• Aspeed AST2600* Advanced PCIe Graphics and Remote Management Processor
	• Embedded features enabled on this server board:
	  o Baseboard Management Controller (BMC)
	  o 2D Video Graphics Adapter

System Configuration and Recovery Jumpers	• BIOS load defaults • BIOS password clear • Intel® Management Engine firmware force update Jumper • BIOS_SVN downgrade • BMC_SVN downgrade

Feature	Details
Security Features	• Intel® Platform Firmware Resilience (Intel® PFR) technology with an I2C interface • Intel® Software Guard Extensions (Intel® SGX) • Converged Intel® Boot Guard and Trusted Execution Technology (Intel® TXT) • Intel® Total Memory Encryption – Multi-Key (Intel® TME-MK) • Trusted platform module 2.0 (China version) – iPC AXXTPMCHNE8 (accessory option) • Trusted platform module 2.0 (rest of the world) – iPC AXXTPMENC9 (accessory option)
Supported Rack Mount Kit Accessory Options **(Sold separately)**	• **CYPHALFEXTRAIL** – Value rack mount rail kit • **CYPFULLEXTRAIL** – Premium rail kit with cable management arm (CMA) support • **AXXCMA2** – CMA (supports **CYPFULLEXTRAIL** only)
BIOS	• Unified Extensible Firmware Interface (UEFI)-based BIOS (legacy boot not supported)

I.2 Intel® Server System M50FCP1UR Family

Power Supply Module
Riser #1 – Add-in Card Area
Interposer Riser – Add-in Card Area
CPU 0
OCP* 3.0 Adapter Area
Riser #2 – Add-in Card Area
CPU 0 EVAC Heat Sink
Riser #3
System Fans
Power Supply Module
Front USB 2.0 Port
OEM Label Pull-Out Tab
CPU 1
Front USB 3.0 Port
System Memory
CPU 1 EVAC Heat Sink
Hot Swap Drive Bays
Chassis
Front Control Panel

Ref #: FCP20221

Riser #2 – Add-in Card Area
Interposer Riser – Add-in Card Area
Riser #1 – Add-in Card Area

Power Supply #1
Video Port (VGA)
Serial Port A (RJ45)
1 GbE Remote Management Port (RJ45)
OCP 3.0 Adapter Area
USB 2.0 Port
USB 3.0 Port
System ID Button w/Integrated LED
Power Supply #2

Ref #: FCP20013

CYP30012

Figure 94. Intel® Server System M50FCP1UR Family

Table 70. Intel® Server System M50FCP1UR Family Features

Feature	Details
Chassis Type	1U rack mount chassis
Chassis Dimensions	767x 438.5 x 43 mm (L x W x H)
Server Board	Intel® Server Board M50FCP2SBSTD

Processor Support	• Dual Socket-E LGA4677
	• Supported 4th Gen Intel® Xeon® Scalable processor family SKUs:
	  ○ Intel® Xeon® Platinum 84xxxx processor
	  ○ Intel® Xeon® Gold 64xxxx processor
	  ○ Intel® Xeon® Gold 54xxxx processor
	  ○ Intel® Xeon® Silver 44xxxx processor
	  ○ Intel® Xeon® Bronze 34xxxx processor
	• Intel® UPI links: 3 at 16 GT/s (Platinum and Gold) or 2 at 16 GT/s (Silver)
	• Intel® Xeon® Bronze processors are used in single processor configurations only.
	Note: Previous generation Intel® Xeon® processor and Intel® Xeon® Scalable processor families are not supported.
	Note: For processor support details, see the *Intel® Server Board M50FCP2SBSTD Technical Product Specification*.

Maximum Supported Processor Thermal Design Power (TDP)	• up to 350W – Intel® Server System M50FCP1UR204 – 4x2.5" Drive Configurations • up to 205W – Intel® Server System M50FCP1UR212 – 12x2.5" Drive Configurations **Note:** The maximum supported processor TDP is dependent on the specific system configuration. Refer to the Intel® Server System M50FCP1UR Technical Product Specification (TPS) for more information.

Chipset	• Intel® C741 chipset platform controller hub (PCH)
	• Embedded features enabled on this server board:
	  ○ SATA 3.0 support
	  ○ USB 3.0 support
	  ○ PCIe 3.0 support

Memory Support	• 32 memory slots:
	  ○ 16 memory slots per processor, eight memory channels per processor
	  ○ Two memory modules per channel
	• Registered DDR5 DIMM (standard RDIMM, 3DS-RDIMM, and 9x4 RDIMM)
	Note: 3DS = 3-dimensional stacking.
	• All DDR5 DIMMs must support ECC
	• Intel® Optane™ PMem 300 series (App Direct Mode only)
	• Memory capacity
	  ○ Up to 12 TB per processor (processor SKU dependent) using DDR5 DIMMs combined with Intel Optane PMem 300 series modules
	• Memory data transfer rates
	  ○ Up to 4800 MT/s at one DIMM per channel (processor SKU dependent)
	  ○ Up to 4400 MT/s at two DIMMs per channel (processor SKU dependent)
	• DDR5 standard voltage of 1.1 V
	Note: For memory support details, see the *Intel® Server Board M50FCP2SBSTD Technical Product Specification*.

System Fan Support	• Eight managed 40-mm hot swap capable system fans • Integrated fans included with each installed power supply module **Note:** System fan redundancy may only be supported on specific system configurations. See the Intel® Server System M50FCP1UR Technical Product Specification (TPS) for more information.

Feature	Details

Power Supply Options	• The server system can support one or two power supply modules configurations.
	• Depending on the power supply configuration, the system will support the following power operating modes:
	  ○ 1+0 – Single functional power supply
	  ○ 1+1 – redundant power
	  ○ 2+0 – combined power, no redundancy
	• Power supply options:
	  ○ AC 1300 W Titanium
	  ○ AC 1600 W Titanium

Server Board Network Support	See optional Open Compute Project (OCP) adapter support.
Open Compute Project* (OCP*) Adapter Support	Server board x16 PCIe 5.0 OCP 3.0 connector (Small Form-Factor) slot. Refer to https://servertools.intel.com/sct for the latest list of adapters supported by the server board.

Riser Card Support	Concurrent support for up to four riser cards, including one PCIe Interposer riser card, with support for up to three PCIe add-in cards. In the following description HL = Half Length, LP = Low Profile.
	Riser Slot #1
	• Riser Slot #1 supports x16 PCIe lanes routed from CPU 0
	• PCIe 5.0 support for up to 32 GB/s
	Riser Slot #1 supports the following Intel riser card option:
	• PCIe slot riser card (iPC **FCP1URISER1**), which supports:
	  ○ One single-width slot (x16 electrical, x16 mechanical)
	Riser Slot #2
	• Riser Slot #2 supports X24 PCIe lanes routed from CPU 1
	• PCIe 5.0 support for up to 32 GB/s
	Riser Slot #2 supports the following Intel riser card options:
	• PCIe slot riser card (iPC **FCP1URISER2**), which supports:
	  ○ One LP/HL, single-width slot (x16 electrical, x16 mechanical)
	• Riser card (iPC **FCP1URISER2KIT**), which supports:
	  ○ One LP/HL, single-width slot (x16 electrical, x16 mechanical)
	  ○ One x8 PCIe MCIO connector with retimer
	PCIe* Interposer Riser Slot (requires PCIe* Riser Card in Riser Slot #2)
	• PCIe interposer riser slot, which supports the PCIe interposer riser card as an accessory option.
	• This card supports one PCIe add-in card (x8 electrical, x8 mechanical).
	• The PCIe interposer riser card can be used only when it is connected to the PCIe riser card in Riser Slot #2. The interposer riser card uses x8 PCIe data lanes routed from the PCIe MCIO connector on the PCIe riser card.
	• The Intel accessory kit (iPC FCP1URISER2KIT) includes the PCIe interposer riser card, PCIe riser card, and PCIe interposer cable.
	Riser Slot #3 **Note:** Riser Slot #3 is not used in the 1U server system.
	• Riser Slot #3 supports x16 PCIe lanes routed from CPU 1
	• PCIe 5.0 support for up to 32 GB/s

PCIe* NVMe* Support	• 16 server board mounted PCIe MCIO connectors, eight per processor (up to 12 used in 1U) • Two M.2 NVMe/SATA connectors • Volume Management Device (VMD) support
Video Support	• Integrated 2D video controller • 128 MB of DDR4 video memory • One VGA connector on the rear of the chassis.

Feature	Details

Server Board SATA Support	• 10 x SATA III ports (6 Gb/s, 3 Gb/s, and 1.5 Gb/s transfer rates supported)
	  ○ Two M.2 connectors: SATA / PCIe
	  ○ Two 4-port Mini-SAS HD (SFF-8643) connectors

USB Support	• One USB 3.0 and two USB 2.0 connectors on the rear of the chassis • One USB 3.0 and one USB 2.0 connector on the front panel
Serial Support	• One external RJ-45 Serial Port A connector on the rear of the chassis
Front Drive Bay Options	• 4 x 2.5" SAS/SATA/NVMe hot swap drive bays (iPC – M50FCP1UR204) • 12 x 2.5" SAS/SATA/NVMe hot swap drive bays (iPC M50FCP1UR212)
Server Management	• Integrated Baseboard Management Controller (BMC) • One dedicated RJ45 1 GbE server management port • Intelligent Platform Management Interface (IPMI) 2.0 compliant • Redfish* compliant • Support for Intel® Data Center Manager (Intel® DCM) • Support for Intel® Server Debug and Provisioning Tool (Intel® SDP Tool) • Integrated BMC Web Console • Intel® Light-Guided Diagnostics • Optional Advanced Server Management features (Purchased separately)
Server Management Processor (SMP)	• Aspeed AST2600* Advanced PCIe Graphics and Remote Management Processor • Embedded features enabled on this server board: • Baseboard management controller (BMC) • 2D video graphics adapter
System Configuration and Recovery Jumpers	• BIOS load defaults • BIOS password clear • Intel® Management Engine (Intel® ME) firmware force update • BIOS_SVN downgrade • BMC_SVN downgrade
Security Features	• Intel® Platform Firmware Resilience (Intel® PFR) technology with an I2C interface • Intel® Software Guard Extensions (Intel® SGX) • Converged Intel® Boot Guard and Intel® Trusted Execution Technology (Intel® TXT) • Intel® Total Memory Encryption – Multi-Key (Intel® TME-MK) • Trusted platform module 2.0 (China version): iPC AXXTPMCHNE8 (accessory option) • Trusted platform module 2.0 (rest of the world): iPC AXXTPMENC9 (accessory option)
Supported Rack Mount Kit Accessory Options	• CYPHALFEXTRAIL – Value rack mount rail kit • CYPFULLEXTRAIL – Premium rail kit with cable management arm (CMA) support • AXXCMA2 – Cable management arm (supports CYPFULLEXTRAIL only)
BIOS	• Unified Extensible Firmware Interface (UEFI)-based BIOS (legacy boot not supported)

Appendix J. Regulatory Information

This product has been evaluated and certified as Information Technology Equipment (ITE), which may be installed in offices, schools, computer rooms, and similar commercial type locations. The suitability of this product for other product certification categories and/or environments (such as: medical, industrial, telecommunications, NEBS, residential, alarm systems, test equipment, and so on), other than an ITE application, requires further evaluation and may require additional regulatory approvals.

Notes:
- An L3 component is a building block option that requires integration into a chassis to create a functional server system.

Intel has verified that all L3, L6, and L9 server products **as configured and sold by Intel** to its customers comply with the requirements for all regulatory certifications defined in the following table. It is the Intel customer's responsibility to ensure that their final server system configurations are tested and certified to meet the regulatory requirements for the countries to which they plan to ship and or deploy server systems into.

	Intel® Server Board M50FCP2SBSTD	Notes
	"Foxcreek Pass"	Intel Project Code Name
	L3 Board	Product integration level
	M50FCP	Product family identified on certification
Regulatory Certification		
RCM DoC Australia & New Zealand	✓	
CB Certification & Report (International - report to include all CB country national deviations)	✓	
China CCC Certification	○	Not required on MB
CU Certification (Russia/Belarus/Kazakhstan)	○	Not required on MB
Europe CE Declaration of Conformity	✓	
FCC Part 15 Emissions Verification (USA & Canada)	✓	
Germany GS Certification	○	Not required on MB
India BIS Certification	○	Not required on MB
International Compliance – CISPR32 & CISPR35	✓	
Japan VCCI Certification	○	Not required on MB
Korea KC Certification	✓	
Mexico Certification	○	Not required on MB
NRTL Certification (USA&Canada)	✓	
South Africa Certification	○	Not required on MB
Taiwan BSMI Certification	✓	DoC for MB
Ukraine Certification	○	Not required on MB

Table Key

Not Tested / Not Certified	○
Tested / Certified – Limited OEM SKUs only	●
Testing / Certification (Planned)	(Date)
Tested / Certified	✓

EU Directive 2019/424 (Lot 9)

Beginning on March 1, 2020, an additional component of the European Union (EU) regulatory CE marking scheme, identified as EU Directive 2019/424 (Lot 9), will go into effect. After this date, all new server systems shipped into or deployed within the EU must meet the full CE marking requirements including those defined by the additional EU Lot 9 regulations.

Intel has verified that all L3, L6, and L9 server products **as configured and sold by Intel** to its customers comply with the full CE regulatory requirements for the given product type, including those defined by EU Lot 9. It is the Intel customer's responsibility to ensure that their final server system configurations are SPEC* SERT* tested and meet the new CE regulatory requirements.

Visit the following website for additional EU Directive 2019/424 (Lot9) information:

https://eur-lex.europa.eu/legal-content/EN/TXT/?uri=CELEX:32019R0424

In compliance with the EU Directive 2019/424 (Lot 9) materials efficiency requirements, Intel makes available all necessary product collaterals as identified below:

- System Disassembly Instructions
  - Intel® Server System M50FCP1UR System Integration and Service Guide
- **Product Specifications**
  - *Intel® Server Board M50FCP2SBSTD Technical Product Specification* (This document)
  - *Intel® Server System M50FCP1UR Technical Product Specification*
- **System BIOS/Firmware and Security Updates – Intel® Server Board M50FCP2SBSTD**
  - System Update Package (SUP) – UEFI only – http://downloadcenter.intel.com
- **Intel® Solid State Drive (SSD) Secure Data Deletion and Firmware Updates**
  Note: For system configurations that may be configured with an Intel® SSD.
  - Intel® Solid State Drive Toolbox: https://downloadcenter.intel.com/product/35125/Memory-and-Storage

- Intel® RAID Controller Firmware Updates and other support collaterals
  Note: For system configurations that may be configured with an Intel® RAID Controller: https://www.intel.com/content/www/us/en/support/products/43732/server-products/raid-products.html

Appendix K. Glossary

Term	Definition
ACPI	Advanced Configuration and Power Interface
ARP	Address Resolution Protocol
ASHRAE	American Society of Heating, Refrigerating, and Air-Conditioning Engineers
ATX	Advanced Technology eXtended
BBS	BIOS boot selection
BMC	Baseboard management controller
BIOS	Basic Input/Output System
CFM	Cubic feet per minute
CLST	Closed loop system throttling
CMOS	Complementary metal-oxide-semiconductor
CPU	Central processing unit
DDR5	Double data rate 5
DHCP	Dynamic Host Configuration Protocol
DIMM	Dual in-line memory module
DPC	DIMMs per channel
DR	Dual rank
EATX	Extended Advanced Technology eXtended
EDS	External design specification
EFI	Extensible firmware interface
FP	Front panel
FRB	Fault resilient boot
FRU	Field replaceable unit
GPGPU	General purpose graphic processing unit
GPIO	General purpose input/output
GUI	Graphical user interface
I²C	Inter-integrated circuit bus
IMC	Integrated memory controller
IIO	Integrated input/output
iPC	Intel® Product Code
IPMI	Intelligent Platform Management Interface
LED	Light emitting diode
LFM	Linear feet per minute, an airflow measurement
LLC	Last level cache
LPC	Low-pin count
LSB	Least significant bit
MCIO	Mini Cool Edge IO
Memory Module	DDR5 DIMM and Intel® Optane™ PMem devices are commonly referred to as "memory module"
MLE	Measured launch environment
MM	Memory mode
MRC	Memory reference code
MSB	Most significant bit
MTBF	Mean time between failure
NAT	Network address translation
NIC	Network interface controller
NMI	Non-maskable interrupt
NTB	Non-transparent bridge
OEM	Original equipment manufacturer
OCP*	Open Compute Project*
OR	Oct rank
OTP	Over temperature protection
OVP	Over-voltage protection
PCH	Peripheral controller hub
PCI	Peripheral component interconnect
PCB	Printed circuit board

Term	Definition
PCIe*	Peripheral Component Interconnect Express*
PFC	Power factor correction
PHM	Processor heat sink module
PMBus*	Power Management Bus*
PMem	Persistent memory, referring to a module.
POST	Power-on self-test
PSU	Power supply unit
PWM	Pulse width modulation
QR	Quad rank
RAID	Redundant array of independent disks
RAM	Random access memory
RAS	Reliability, availability, and serviceability
RCiEP	Root complex integrated endpoint
RDIMM	Registered DIMM
RMCP	Remote Management Control Protocol
ROC	RAID on CPU
SAS	Serial Attached SCSI
SATA	Serial Advanced Technology Attachment
SEL	System event log
SCA	Single connector attachment
SCSI	Small Computer System Interface
SDR	Sensor data record
SFF	Small form factor
SFP	Small form-factor pluggable
SFUP	Single boot firmware update package
Intel® SGX	Intel® Software Guard Extensions
SMBus	System Management Bus
SMP	Server management processor
SMTP	Simple Mail Transfer Protocol
SNMP	Simple Network Management Protocol
SOL	Serial-over-LAN
sSATA	Secondary SATA
SR	Single rank
SSD	Solid state drive
TCG	Trusted Computing Group
TDP	Thermal design power
TIM	Thermal interface material
Intel® TME	Intel® Total Memory Encryption (Intel® TME)
Intel® TME-MK	Intel® Total Memory Encryption – Multi-Key (Intel® TME-MK)
TPM	Trusted platform module
TPS	Technical product specification
Intel® TXT	Intel® Trusted Execution Technology
UEFI	Unified Extensible Firmware Interface
Intel® UPI	Intel® Ultra Path Interconnect
VLSI	Very large scale integration
VMD	Volume Management Device
VSB	Voltage standby
Intel® VT-d	Intel® Virtualization Technology for Directed I/O
Intel® VT-x	Intel® Virtualization Technology for IA-32, Intel® 64 and Intel® Architecture